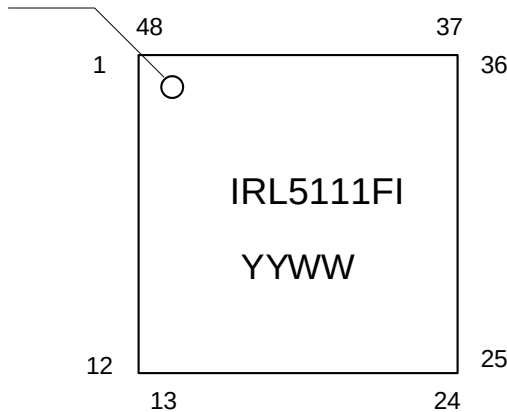


8-Channel 12-Bit ADC with Bipolar Input Range

the 1st pin
indicator



YY – Year of manufacture
WW – Week of manufacture

Features:

- 12-Bit ADC with Integrated Analog Input Stages;
- 8-Channel Multiplexer with Automatic and Manual Scanning Modes;
- Single-Ended and Differential Input Signal Processing;
- Independently programmable input range for each channel:
 - ± 10.24 V, ± 5.12 V, ± 2.56 V, ± 1.28 V, ± 0.64 V;
 - 10.24 V, 5.12 V, 2.56 V, 1.28 V, 0.64 V (0.64 V only in differential mode);
- Unipolar supply voltage:
 - 5 V for the analog section;
 - from 1.8 to 5 V for the digital interface;
- Resistive input impedance greater than 1 M Ω ;
- Overvoltage protection up to ± 20 V;
- Built-in 4.096 V voltage reference with low drift;
- Built-in oscillator;
- Total throughput of 500 kSPS/s;
- DNL: ± 0.2 LSB; INL: ± 0.75 LSB
- SNR: 72.5 dB; SFDR: 80 dB;
- Supply current: 1 mA/channel;
- Direct access to the ADC via the AUX input;
- Serial SPI interface with Daisy Chain support;
- Alarm function with a programmable threshold for each channel;
- Operating temperature range: from minus 40 °C to plus 85 °C.

Package type:

- 48-pin plastic package QFN48.

The mass of the integrated circuits is no more than 0.2 g.

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1 General description and application areas of the integrated circuit

The IRL5111FI are 8-channel integrated data acquisition systems based on a 12-bit ADC successive approximation, capable of outputting digital reports with a throughput of 500 ksamples/s and minimal latency (hereinafter referred to as the integrated circuits). The integrated circuits include eight analog signal conditioning chains (hereinafter – channels) with overvoltage protection at the input up to ± 20 V, a multiplexer with automatic or manual scanning, and a built-in voltage reference of 4.096 V. The integrated circuits operate from a unipolar supply voltage of 5 V, while each channel can be individually programmed to operate with bipolar input ranges from ± 0.64 to ± 10.24 V in differential or single-ended modes, or unipolar ranges from 0 to 1.28 – 10.24 V in single-ended or from 0 to 0.64 – 10.24 V in differential mode. The gain and zero offset of each channel are adjusted during manufacturing to improve processing accuracy. The integrated circuits feature high input impedance, independent of frequency.

Collection of output digital data and control of the integrated circuits' modes are performed through a simple serial interface SPI. Support for connecting multiple integrated circuits in a common chain for synchronous collection of output samples (Daisy Chain). The digital supply voltage of the integrated circuits can vary from 1.65 to 5.25 V, allowing direct connection to digital controllers and FPGAs with various logic levels and PLDs.

The integrated circuits are intended for use in modern control systems, automation, and measurement systems, as well as in any other devices that can receive and process ADC samples.

2 Microchip block diagram

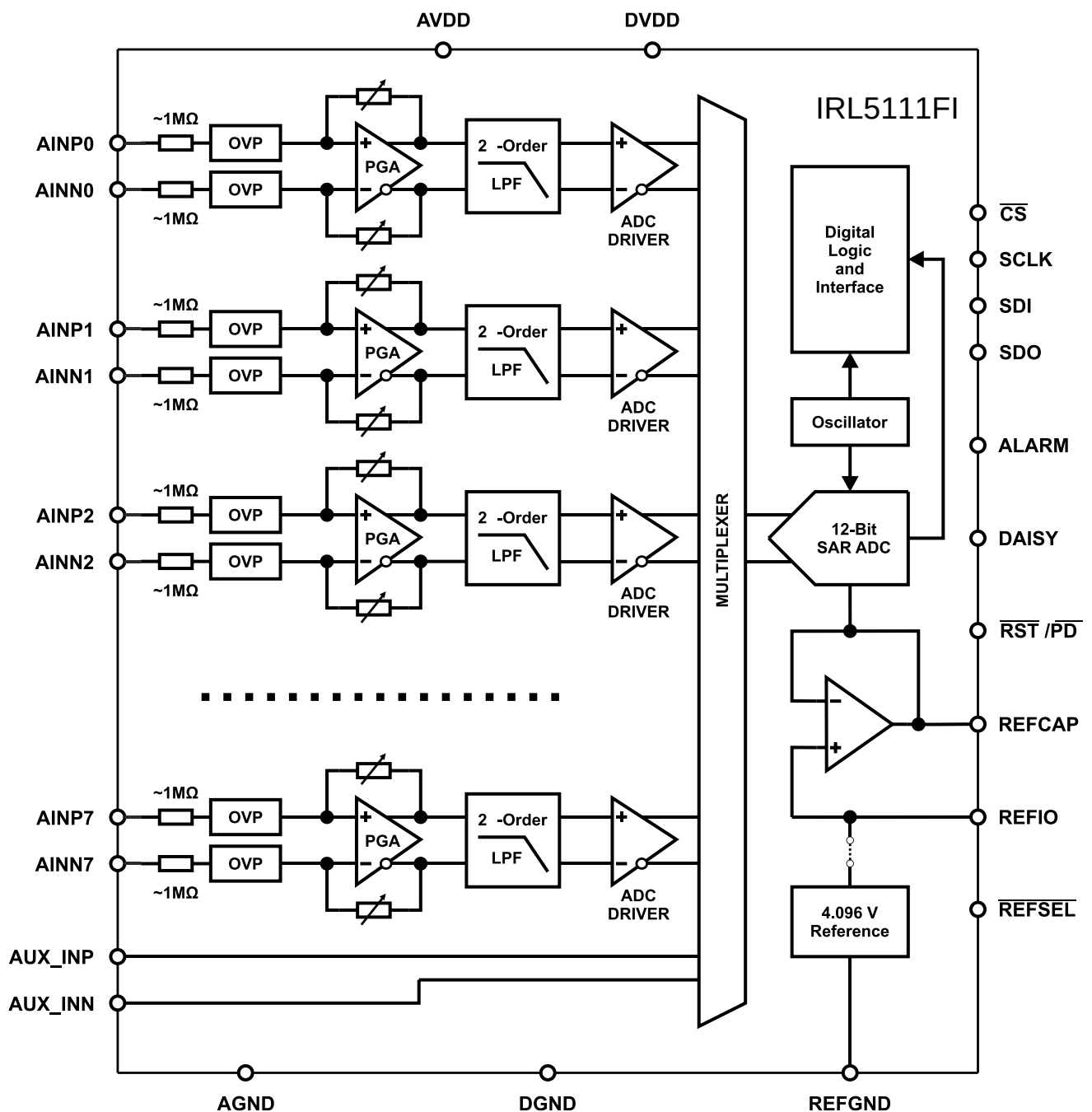


Figure 1 – Block diagram

3 Conditional graphic symbols

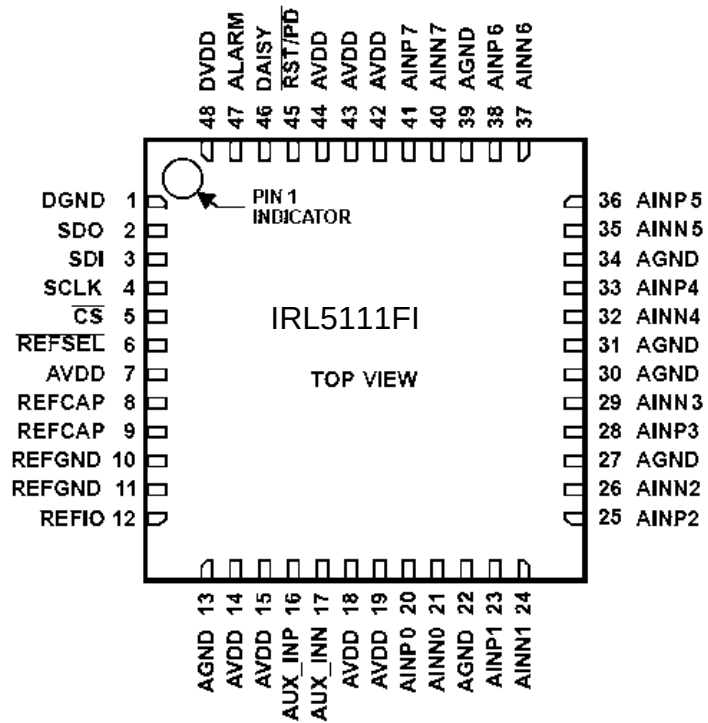


Figure 2 – Conditional graphic symbol for IRL5111FI

4 Pin description

Table 1 – Microchip pin description

Pin number	Pin designation	Pin type	Pin function
3	SDI	I	Serial interface data input
45	nRST/nPD	I	Reset of all memory elements and restart or disable of the device: - short "0" - reset state; - long "0" - off mode followed by reset; - "1" - "Normal" mode
46	DAISY	I	Data input for serial connection of multiple devices in a chain. Connect to common GND if Daisy Chain is not used
6	nREFSEL	I	Configuration of the internal voltage reference: - "0" - internal reference enabled (REFIO becomes an output, on which the V_{REF} voltage is established); - "1" - internal reference disabled (REFIO becomes an input, to which an external V_{REF} voltage must be applied)
12	REFIO	AIO	Internal reference voltage output or external reference voltage input. (Install a filter capacitor to REFGND)
10, 11	REFGND	PWR	Common. (Place as close as possible to the common GND plane, install a filter capacitor between REFIO and REFCAP)
8, 9	REFCAP	AO	ADC reference voltage filter capacitor. (Install a filter capacitor to REFGND)
7, 14, 15, 18, 19, 42-44	AVDD	PWR	Analog power supply. (Place a filter capacitor on AGND)
16	AUX_INP	AI	Non-inverting ADC input bypassing the AFE
17	AUX_INN	AI	Inverting ADC input bypassing the AFE
20	AINP0	AI	Non-inverting input of channel 0
21	AINN0	AI	Inverting input of channel 0
23	AINP1	AI	Non-inverting input of channel 1
24	AINN1	AI	Inverting input of channel 1
25	AINP2	AI	Non-inverting input of channel 2
26	AINN2	AI	Inverting input of channel 2
28	AINP3	AI	Non-inverting input of channel 3
29	AINN3	AI	Inverting input of channel 3
33	AINP4	AI	Non-inverting input of channel 4
32	AINN4	AI	Inverting input of channel 4
36	AINP5	AI	Non-inverting input of channel 5
35	AINN5	AI	Inverting input of channel 5
38	AINP6	AI	Non-inverting input of channel 6
37	AINN6	AI	Inverting input of channel 6

Pin number	Pin designation	Pin type	Pin function
41	AINP7	AI	Non-inverting input of channel 7
40	AINN7	AI	Inverting input of channel 7
48	DVDD	PWR	Digital power supply. (Connect a filter capacitor to DGND)
1	DGND	PWR	Common, digital. Connect to the common GND
47	ALARM	O	Output of the Alarm function
2	SDO	O	Serial interface data output
4	SCLK	I	Serial interface synchronization input
5	nCS	I	Serial interface selection (if SPI is not used – “1”), ADC sample signal
13, 22, 27, 30, 31, 34, 39, 0 (backside metallization of the package)	AGND	PWR	Common, analog. Connect to the common GND
Note – Pin type designations: PWR – power supply and common; I – digital input; O – digital output; IO – digital input / output; AI – analog input; AO – analog output; AIO – analog input / output			

5 Application and Operation Guidelines

When servicing equipment and measuring parameters, integrated circuits must be replaced only with the power supplies disconnected.

It is prohibited to apply any electrical signals (including power supply buses and ground) to the pins of integrated circuits that are not used according to the electrical schematic.

The typical circuit for connecting integrated circuits is shown in Figure 16.

The sequence for applying and removing supply voltages and input signals to the integrated circuits shall be as follows:

- a) application (turning on the integrated circuit):
 - 1) common;
 - 2) simultaneous power supply of the digital interface and analog blocks;
 - 4) input signal to the nRST/nPD pin, if required;
 - 5) programming of the SPI interface, if required;
 - 6) external reference voltage (if required);
 - 7) input signals;
- b) removal (chip shutdown):
 - 1) input signals in reverse order;
 - 2) supply simultaneously;
 - 3) common.

6 Chip operation description

6.1 Structure and general description of the chip

The IRL5111FI devices are 12-bit data acquisition and digitization systems with an 8-channel analog input (see Figure 1). Each channel consists of an overvoltage protection circuit (OVP), a programmable gain amplifier (PGA), a second-order anti-aliasing filter (LPF) and an ADC driver buffer, the output of which is connected to an 8-channel analog multiplexer. The multiplexer output signal is processed by a 12-bit analog-to-digital converter (ADC) implemented using a successive approximation architecture. The ADC conversion rate is sufficient to ensure the throughput of the entire system 500 kSps/s, taking into account the time required for the serial output of digital samples. The devices also include a buffered 4.096 V voltage reference and a simple-to-control digital serial interface (SPI) with Daisy Chain and Alarm functions. Figure 1

The device operates from a single 5 V supply, but is capable of accepting bipolar input signals up to $\pm 2.5 \cdot U_{REF}$, in both single-ended and differential modes. The input impedance of the devices is constant, approximately 1 M Ω , with weak dependence on frequency and input range.

This multi-channel analog signal pre-processing circuit offers high accuracy and, when combined with the integrated ADC, can significantly simplify application development, as it does not require external high-voltage buffers or complex drivers with bipolar power supplies.

6.2 Pre-processing of the analog input signal

The IRL5111FI devices feature eight analog channels. The AINPx ($x = 0 \dots 7$) inputs are intended for applying the single-ended analog signal to be processed, or its non-inverting phase in differential mode. Correspondingly, the AINN x inputs are either tied to ground or receive the inverting phase of the differential signal.

6.2.1 Operating ranges

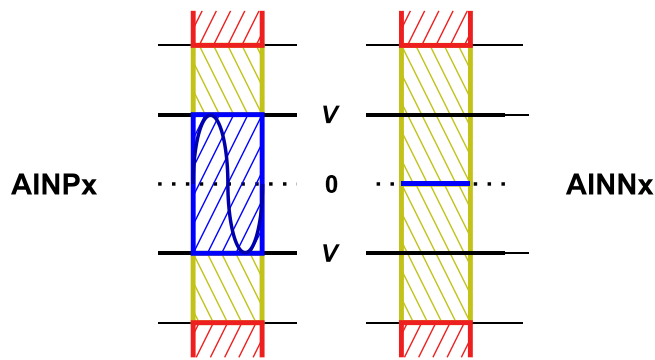
The device supports various ranges and modes for input analog signals. Depending on the current channel settings in single-ended mode, the permissible voltages at the AINPx inputs may be bipolar $\pm 2.5 \cdot U_{REF}$, $\pm 1.25 \cdot U_{REF}$, $\pm 0.625 \cdot U_{REF}$, $\pm 0.3125 \cdot U_{REF}$, $\pm 0.15625 \cdot U_{REF}$ or unipolar ranges from 0 to $2.5 \cdot U_{REF}$, from 0 to $1.25 \cdot U_{REF}$, from 0 to $0.625 \cdot U_{REF}$ and from 0 to $0.3125 \cdot U_{REF}$. For the AINN x inputs in single-ended mode, a “0” must be applied for any of the listed configurations.

In differential mode, the following ranges are possible for each of the AINPx, AINN x : bipolar $\pm 1.25 \cdot U_{REF}$, $\pm 0.625 \cdot U_{REF}$, $\pm 0.3125 \cdot U_{REF}$, $\pm 0.15625 \cdot U_{REF}$, $\pm 0.078125 \cdot U_{REF}$ or unipolar ranges from 0 to $2.5 \cdot U_{REF}$, from 0 to $1.25 \cdot U_{REF}$, from 0 to $0.625 \cdot U_{REF}$ and from 0 to $0.3125 \cdot U_{REF}$.

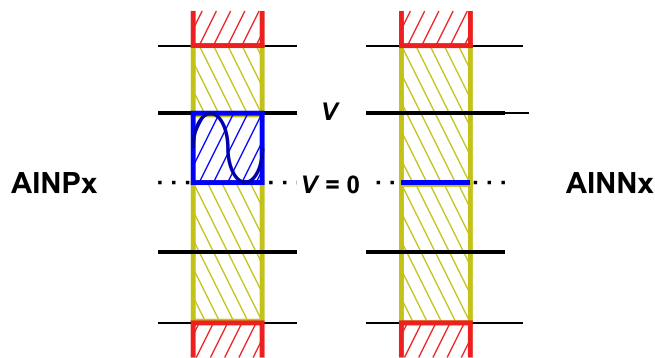
With an internal or external reference voltage of $U_{REF} = 4.096 \text{ V}$, the limits of the permissible input ranges U_T and U_B take the values indicated on the left side of Figure 3 – Maximum permissible and limit input ranges ($U_{REF} \ll 93$. Any of these ranges can be individually defined for each of the eight channels.

In any mode, the ADC samples the voltage between the AINPx and AINN x inputs. In single-ended mode, a deviation of AINN x of $\pm 0.1 \text{ V}$ relative to the chip's common ground is permissible. This feature is useful in systems where electronic modules are located at a significant distance from each other, and where a significant potential difference between the grounds of the analog signal source and the IRL5111FI is not excluded. In this case, it is recommended to run a separate metal line from the ground of the single-ended source to the AINN x pin. If the analog signal source supports a differential configuration, it is better to use it, connecting the source outputs to the AINPx and AINN x pins.

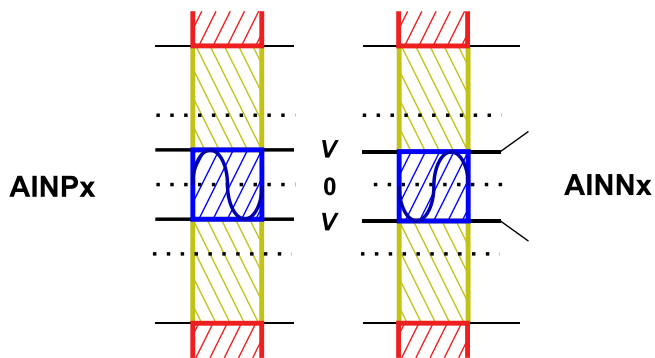
If a connection to any of the AINPx/AINN x inputs is broken during operation, this will not damage the chip. However, the code at the ADC output will be incorrect until valid voltages are applied to the analog inputs.



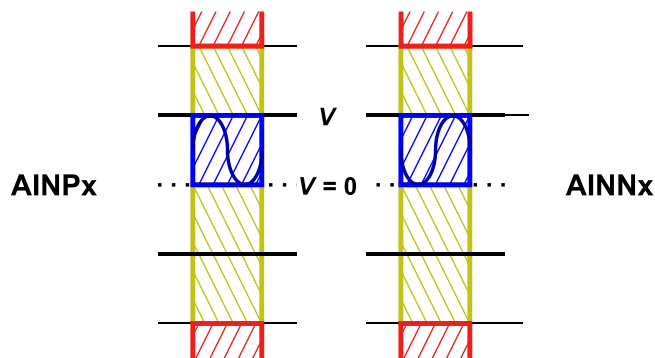
Bipolar Range, Single-Ended Mode ($nD=1$; $U=0$)



Unipolar Range, Single-Ended Mode ($nD=1$; $U=1$)



Bipolar Range, Differential Mode ($nD=0$; $U=0$)



Unipolar Range, Differential Mode ($nD=0$; $U=1$)

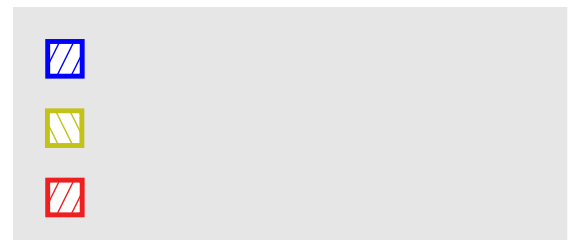


Figure 3 – Maximum permissible and limit input ranges ($U_{REF}=4.096V$)

6.2.2 Input impedance

The input impedance of each AINPx and AINN_x pin is a constant resistive impedance of greater than 1 MΩ, which is independent of the ADC sampling frequency or the input signal frequency.

The high input impedance of the IRL5111FI significantly simplifies interface with the ADC, as there is no need for an external low-output-impedance buffer, nor for bipolar high-voltage supply. In most applications it allows to apply the analog input signal directly to the device from a source or sensor.

To improve operating accuracy, it is recommended that the output impedance of the analog signal source at the AINPx pin be as close as possible to the impedance at the AINN_x pin, as their mismatch may cause zero offset in the system.

6.2.3 Overvoltage protection circuitry

For each analog AINPx and AINN_x input in the IRL5111FI, a protection circuit is provided to prevent device damage in the event of high voltage occurrence on these pins. This protection should be considered secondary, in addition to other external devices for protection against voltage spikes, electrostatic discharge (ESD), and electrical fast transients (EFT).

As shown in the equivalent circuit in Figure 4, the combination of the 1 MΩ input resistor and the feedback resistor of the programmable amplifier limits the current flowing into the analog inputs. The Zener diodes DZ1 and DZ2 protect the internal circuitry and, together with the electrostatic discharge protection (ESD), determine the maximum overvoltage level $U_{OVP} = 20\text{ V}$.

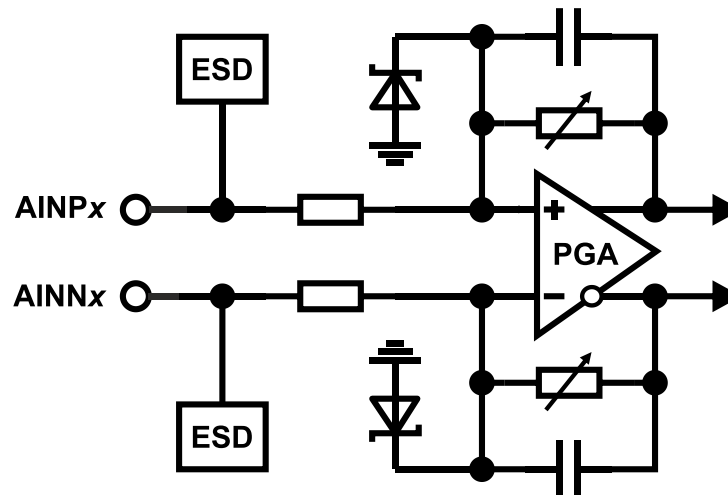


Figure 4 – Input stage equivalent circuit

Figure Figure 3 – Maximum permissible and limit input ranges ((UREF[93 shows the conditions under which the channel operates in normal processing mode and the conditions under which overvoltage protection is provided :

- As long as the voltages on the analog pins U_{IAP} and U_{IAN} are within the operating range (blue area), i.e., $U_B \leq U_{IAP}$, $U_{IAN} \leq U_T$, correct analog-to-digital conversion is performed .
- If the input voltage exceeds the operating range but remains within the protection range (yellow area), i.e., $-U_{OVP} \leq U_{IAP}$, $U_{IAN} \leq U_{OVP}$, the ADC output saturates. Although the device remains functional, it is not recommended to intentionally keep it in this state for extended periods.
- If the protection range is exceeded (red area), irreversible damage to the device may occur.

The specified U_{OVP} values apply to a very low, near-zero output impedance of the analog signal source R_s . If the analog signal is sourced from a higher-impedance source, the input current will be further limited, which increases the protection range U_{OVP} . However, note that increasing R_s results in gain error (see Figure 17) and increased system noise.

The built-in overvoltage protection is also effective if input signals are already present at the device while the supply voltage has not yet been applied.

6.2.4 Programmable Gain Amplifier

The input stage of each channel is a programmable gain amplifier (PGA). Its primary function is to scale the input signal relative to the ADC range to achieve maximum dynamic range. The amplifier also converts a single-ended signal to a differential signal with an optimal common-mode level for the ADC.

To set the operating input range for a given channel, the corresponding Channel Input Range register must be programmed (see Table 5). In the GAIN fields, set the required PGA gain, in the nD field, specify whether it operates in single-ended or differential mode and with which signal type – bipolar or unipolar (bit U). The programmable channel number is set by the least significant *Channel* field. All possible options are listed in the summary Table 2.

The amplifier uses well-matched resistor ladders, which are trimmed for each channel during manufacturing to reduce total gain error.

Table 2 – Setting the input operating range

Input analog signal range	U_B , V	U_T , V	PGA gain factor PGA	EMR magnitude, mV	GAIN	nD	U
$\pm 2.5 \cdot U_{REF}$ single-wire;	-10,24	10,24	0,4	5	000	1	0
$\pm 1.25 \cdot U_{REF}$ single-wire;	-5,12	5,12	0,8	2,5	001	1	0
$\pm 0.625 \cdot U_{REF}$ single-wire;	-2,56	2,56	1,6	1,25	010	1	0
$\pm 0.3125 \cdot U_{REF}$ single-wire;	-1,28	1,28	3,2	0,625	011	1	0
$\pm 0.15625 \cdot U_{REF}$ single-wire;	-0,64	0,64	6,4	0,313	100	1	0
0 to $2.5 \cdot U_{REF}$ single-ended;	0	10,24	0,4	2,5	000	1	1
0 to $1.25 \cdot U_{REF}$ single-ended;	0	5,12	0,8	1,25	001	1	1
0 to $0.625 \cdot U_{REF}$ single-ended;	0	2,56	1,6	0,625	010	1	1
0 to $0.3125 \cdot U_{REF}$ single-ended;	0	1,28	3,2	0,313	011	1	1
$\pm 1.25 \cdot U_{REF}$ differential;	-5,12	5,12	0,4	5	000	0	0
$\pm 0.625 \cdot U_{REF}$ differential;	-2,56	2,56	0,8	2,5	001	0	0
$\pm 0.3125 \cdot U_{REF}$ differential;	-1,28	1,28	1,6	1,25	010	0	0
$\pm 0.15625 \cdot U_{REF}$ differential;	-0,64	0,64	3,2	0,625	011	0	0
$\pm 0.078125 \cdot U_{REF}$ differential;	-0,32	0,32	6,4	0,313	100	0	0
from 0 to $2.5 \cdot U_{REF}$ differential;	0	10,24	0,4	5	000	0	1
from 0 to $1.25 \cdot U_{REF}$ differential;	0	5,12	0,8	2,5	001	0	1
from 0 to $0.625 \cdot U_{REF}$ differential;	0	2,56	1,6	1,25	010	0	1
from 0 to $0.3125 \cdot U_{REF}$ differential;	0	1,28	3,2	0,625	011	0	1
from 0 to	0	0,64	6,4	0,313	100	0	1

0.15625·U _{REF} differential;				
Note – The values of U _B , U _T and EMR are given for U _{REF} = 4.096 V				

6.2.5 Anti-aliasing filter

Each AFE channel of the AFE contains a low-pass filter that reduces the noise of the analog signal fed to the ADC. The anti-aliasing filter is second-order with a -3-dB cutoff frequency of 15 kHz. Due to the filter design, the dynamic characteristics of the channel (SFDR, SNDR, etc.) begin to degrade when processing input signals with frequencies above 2 kHz.

The amplitude and phase frequency response of the entire channel, due to the presence of the filter, is as shown in Figure 22. Figure 22 – Amplitude-frequency and phase--frequency characteristics of the channel for input ranges in nD=1 (single-ended), U=0 (bipolar) mode22

6.2.6 ADC Driver

To achieve the specified conversion characteristics at maximum speed, the sampling capacitors at the ADC inputs must be charged by the end of the sampling time. This task is performed by a wideband low-noise amplifier integrated into each input signal preprocessing channel. When switching between channels, this ADC driver amplifier ensures that the multiplexer output also settles to 12-bit accuracy within the sampling time, regardless of the levels at the inputs of these channels.

6.2.7 Multiplexer

The IRL5111FI microchips include an eight-channel analog multiplexer, whose inputs receive the channel input signals that have passed through the preprocessing path. The multiplexer output is directly connected to the ADC.

The multiplexer can scan the analog inputs AINPx/AINN_x either in manual or automatic mode, as described in Section 6.6.2.

6.3 Voltage reference

To set the ADC scale, either an internal or an external voltage reference can be used. In either case, this voltage is pre-buffered inside the die to achieve maximum ADC performance. The selection between the internal and external voltage reference is made using the nREFSEL pin.

6.3.1 Internal reference voltage

The internal reference voltage of nominal value 4.096 V is active when nREFSEL is pulled to AGND. In this case, the REFIO pin becomes an output and is connected to the output of the internal voltage reference. It is recommended to place a filter capacitor of at least 10 μ F (with an equivalent series resistance $ESR \leq 5 \Omega$) between the REFIO and REFGND pins. The capacitor should be placed as close to REFIO as possible. The output impedance of the voltage reference together with this capacitor forms a low-pass filter and limits the noise of the reference voltage. Using capacitors with a lower value may degrade the signal-to-noise ratio of the system. The REFIO output has weak load capability and must not be used to power external circuits without additional buffering.

The internal reference voltage is trimmed during manufacturing with an accuracy of ± 2 mV. However, deviation from the specified accuracy is possible in the final product due to mechanical and thermal stresses during packaging and PCB mounting.

The internal voltage reference includes a temperature compensation circuit to minimize drift over a wide temperature range.

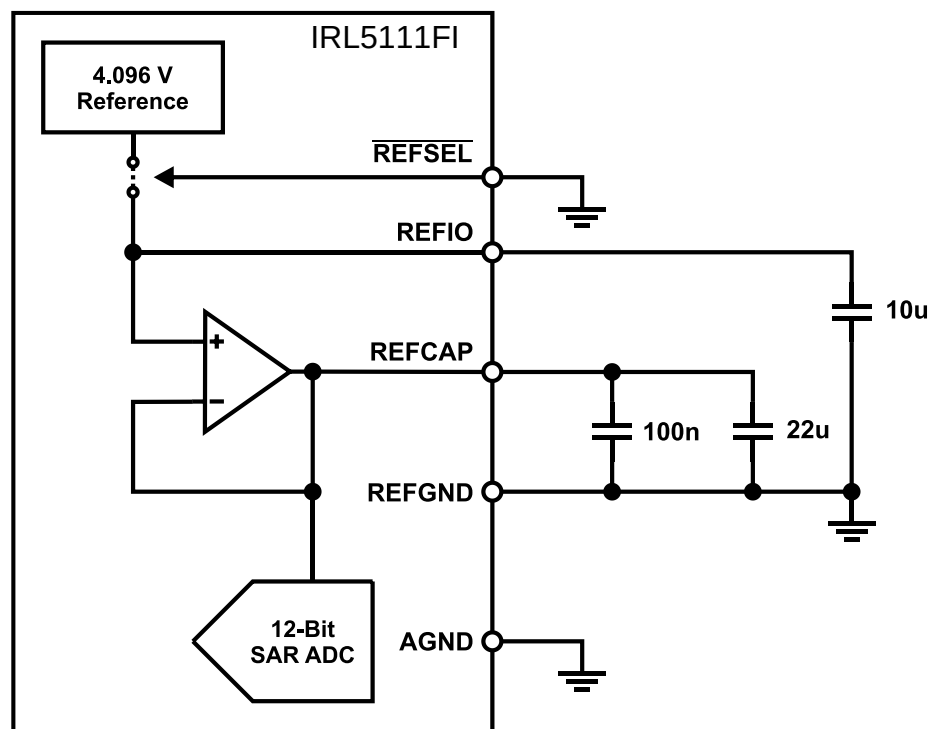


Figure 5 – Equivalent circuit for operation from the internal voltage reference

6.3.1 External reference voltage

In applications requiring a more accurate reference voltage or using a common reference voltage for multiple devices, the capability of the IRL5111FI to operate with an external voltage reference can be utilized. To switch to external reference voltage mode, the nREFSEL pin must be connected to DVDD. In this mode, an external reference voltage of 4.096 V must be applied to the REFIO pin, which becomes an input.

The external voltage reference does not require high current drive capability, as the reference voltage is buffered internally before being applied to the ADC. The external voltage reference supply line must be properly filtered (capacitor C_{REF} in Figure 6), to minimize its impact on the system's noise characteristics.

The output of the internal reference voltage buffer is connected to the REFCAP pin. A capacitor with a value of 22 μ F (with an equivalent series resistance $ESR \leq 1.5 \Omega$, for example, a tantalum capacitor) must be placed as close as possible to the REFCAP and REFGND pins, and in parallel with it, a 100 nF ceramic capacitor for filtering high-frequency noise on the ADC reference voltage. Excessive series resistance (including ESR) between these capacitors and the REFCAP pin causes sharp "spikes" in the internal reference voltage at the start and end of conversion, which in turn degrades system performance.

The internal reference voltage buffer should not be used to power external circuits, as its current drive capability is limited.

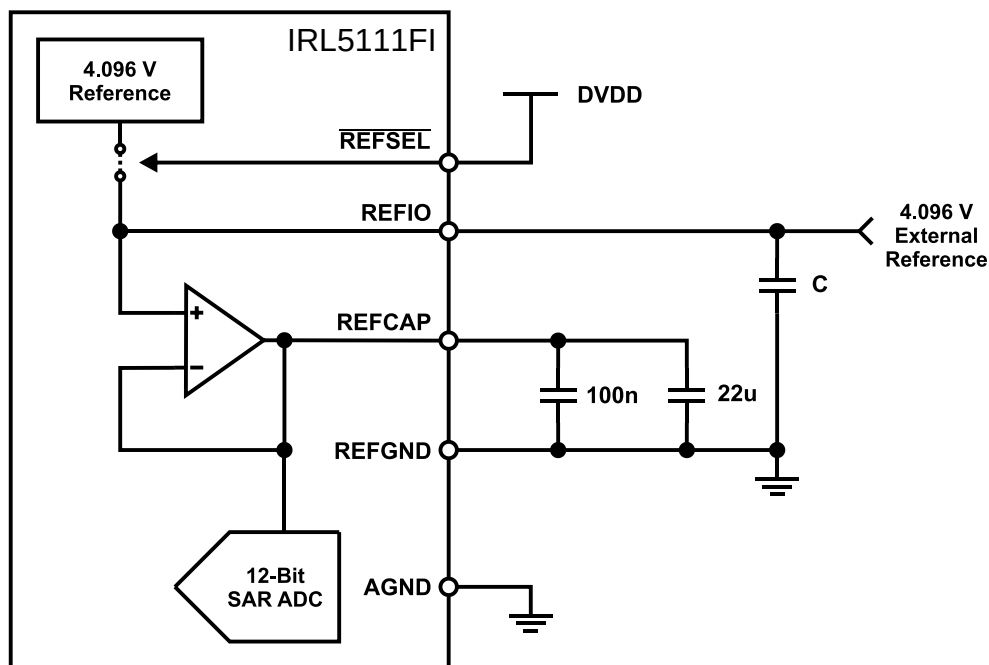


Figure 6 – Equivalent circuit for operation from an external voltage reference

6.4 Analog-to-digital converter

6.4.1 ADC transfer function

The IRL5111FI devices support bipolar, unipolar, differential, and single-ended input ranges on all channels. The ADC digital output format is identical for all ranges – binary code.

The ideal ADC transfer characteristic is shown at the top of Figure 7. The values V_B , V_T , LSB in the figure correspond to the parameters U_B , U_T , EMP in Table 2. The middle and bottom parts of Figure 7 illustrate how the static errors of the ADC are calculated: gain error (GE), offset error (OFF), integral nonlinearity (INL) and differential nonlinearity.

6.4.2 Direct access to the ADC via the AUX-pin

The IRL5111FI devices include a direct access channel to the ADC via the AUX_INP/AUX_INN . A differential or single-ended analog signal is applied to the multiplexer and then to the ADC, bypassing the preprocessing path. In the absence of a PGA, the input signal on the AUX_INP pin can vary from 0 to U_{REF} , while on the AUX_INN – pin it can vary from 0 to U_{REF} in differential mode and only 0 in single-ended mode. Selection between these modes is performed using the SE bit of the Feature *register*: “1” – single-ended, “0” – differential mode.

At the moment of conversion initialization, the voltage difference between these two pins is sampled directly onto the internal sampling capacitor (approximately 15 pF). The current required to charge this capacitor is determined by several factors, including the conversion frequency, and the output impedance of the analog input signal source. For slow applications using a low-impedance source, direct connection to the ADC is acceptable. In other cases, an additional buffer amplifier capable of charging the internal capacitor within the sampling time must be installed.

Digitization of the analog signal on the pins AUX_INP/AUX_INN is performed after transitioning to the MANAUX state.

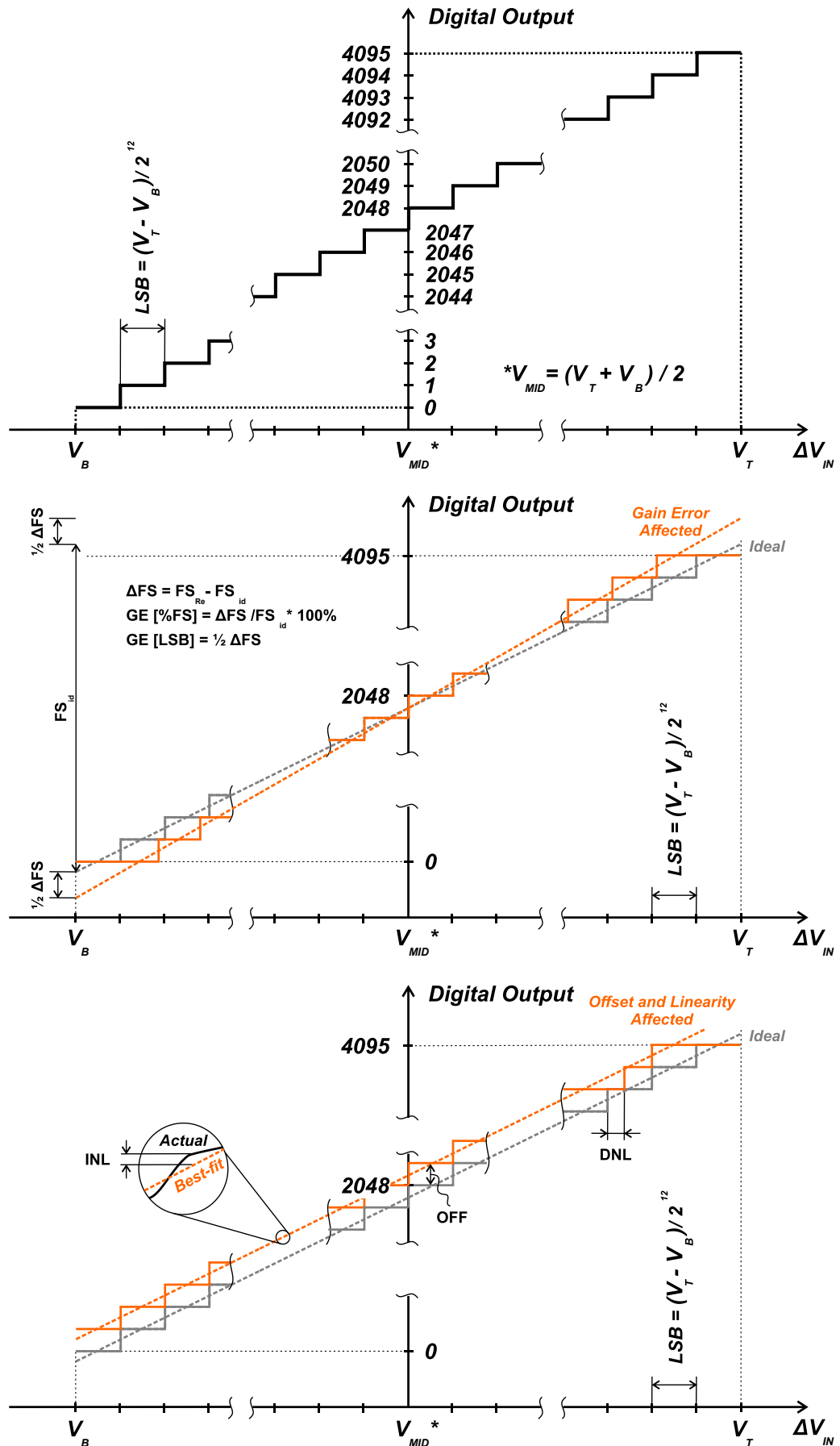


Figure 7 – ADC transfer function and its errors

6.5 Reset and power modes

The IRL5111FI devices can be reinitialized and/or switched to a low-power mode by hardware or software means. Hardware reset or device shutdown is performed via the nRST/nPD pin, as shown in Figure 8. These and other reset and power-down options are summarized in Table 3.

To reduce power consumption in normal operating mode, unused channels can be disabled. To do this, set '1' in the bits corresponding to the channels to be disabled in the *Channel Power Down* (Table 5) register. The disabled channels must also be excluded from the automatic scan list by writing '0' to the corresponding bits of the *Auto Sequence* register, because the *Auto Sequence* register takes precedence over *Channel Power Down* even for a single analog-to-digital conversion. In automatic channel scan mode, only those channels specified in the *Channel Power Down* register and not included in the scan sequence remain disabled.

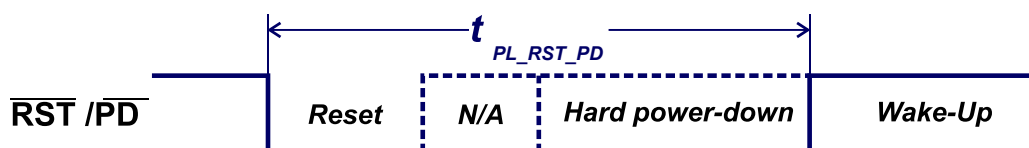


Figure 8 – Timing diagram of the nRST/nPD control signal

Table 3 – Description of chip reset options and power modes

Reset option	Description	Condition			Output time
Hardware reset	Full reinitialization: all registers, including trims, are returned to their initial state; internal memory is read	Power-up or Low level on the nRST/nPD pin for a duration of 40 ns < t _{PL_RST_PD} < 300 ns			~ 10 ms
Software reset	Reinitialization of all registers except trims	The 16th falling edge of SCLK of any command (for example, NOP) executed in the INIT			~ 1 μs
Power mode	Description	Input	Output	Supply current	Output time
Hardware "off" mode	Disabling of all internal blocks and hardware reset	A low level on the nRST/nPD pin with a duration of t _{PL_RST_PD} > 1 μs	A high level on the nRST/nPD	~ 0.7 μA	~ 15 ms
Programmed "off" mode	Disabling all internal blocks except the power monitor	PWRDN state	Transition to any other state	~ 3 μA	~ 15 ms
Wait mode	Voltage reference generation blocks are not disabled	STDBY state	Transition to any other state	~ 0.5 mA	~ 100 μs
Normal mode	All blocks enabled	All states except PWRDN, STDBY	-	-	-

6.6 Control via the serial interface

Configuration of the IRL5111FI device, as well as starting and obtaining the result of the analog-to-digital conversion, is performed through a four-wire SPI interface. The timing diagram of its operation is shown in Figure 9.

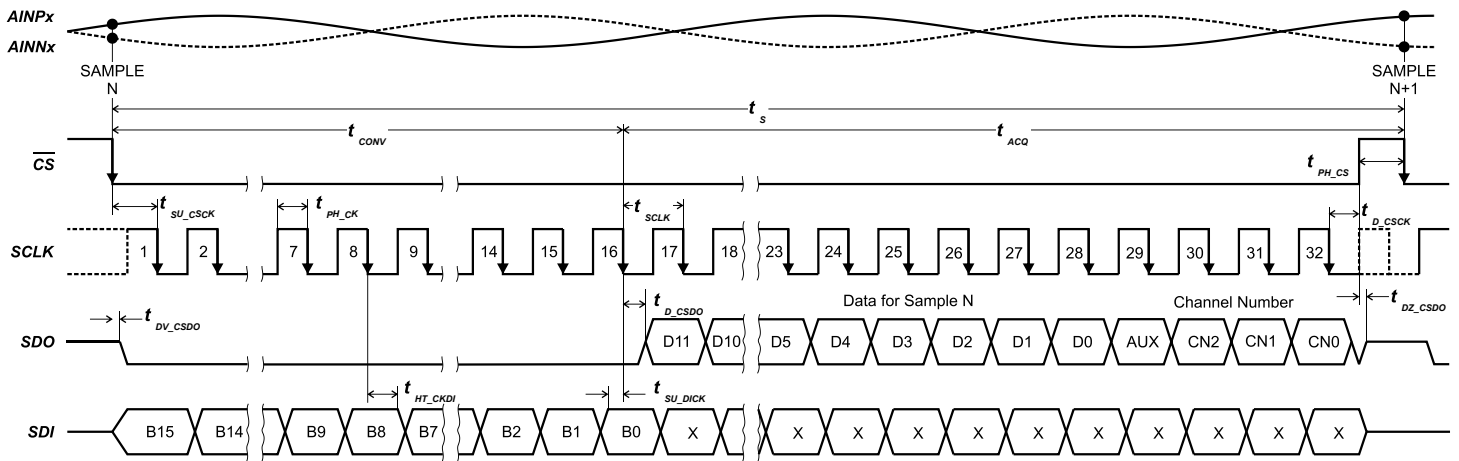


Figure 9 – Serial interface timing diagram

6.6.1 Analog-to-digital conversion

Sampling of the analog signal in the ADC is performed on the falling edge of the nCS signal nCS. Although the subsequent processing of this sample using the successive approximation algorithm is driven by an internal clock signal, pulses must be applied to the SCLK pin. If the frequency of these pulses does not exceed the allowable values, then by the 16th falling edge of SCLK the analog-to-digital conversion is guaranteed to be complete, and the most significant bit of the SDO result is output on the pin. On the subsequent falling edges of SCLK the remaining bits of this digital report are output sequentially and, at the end, starting from the 28th clock cycle – the number of the channel to which it corresponds or other additional information, depending on the current settings.

Special requirements are imposed on the falling edge jitter of the nCS signal, as it determines the sampling instant. In the case of streaming a sinusoidal signal, the jitter on this nCS falling edge must be minimized.

On the 16th falling edge of SCLK simultaneously with the start of the bit-by-bit transmission of the current digital report, the sampling phase of the next report begins – the ADC input switches are opened for charging of the internal capacitor matrix, which continues until the next falling edge of nCS. The minimum duration of the sampling phase is limited (see Table 7), while the maximum is not. To increase the sampling time, it is sufficient to delay the next SPI transaction. A longer sampling time may be required, for example, in case of a sharp change in the analog signal at the input of the pre-processing channel. Since its bandwidth is approximately 15 kHz, a time of about 300 μ s will be required in this case for the signal to fully settle at the ADC input.

6.6.2 Initiating analog-to-digital conversion

Once the input operating ranges are defined (see Section 6.2.4) and the required channels are enabled (see Section 6.5), analog-to-digital conversion of the voltages at their inputs can be performed.

To initiate a single analog-to-digital conversion, the device must first be placed in the MANCH state by applying the corresponding command with the channel number specified (see Table 4). After this, the conversion can be initiated either by repeating the MANCH

command or by the NOP command. If it is necessary to digitize the signal in direct ADC access mode (AUX), the MANAUX command is used instead of the MANCH command.

In applications where a specific set of channels needs to be polled regularly, analog-to-digital conversion can be initiated with automatic channel scanning. For the channels of interest, set '1' in the mask bits of the Auto Sequence register (Table 5), and then use the AUTO or AUTOR command (Section 6.6.4). Since each conversion requires an SPI transaction, the simplest method is to send NOP commands as many times as required for polling. The multiplexer switches channels in ascending order, starting from the lowest number (AUTOR), or resumes scanning from the channel where the cycle was stopped last time (AUTO).

6.6.3 Features of the SPI interface

- All changes occur on the falling edge of SCLK. The state of SCLK at the beginning of the frame (nCS transitions from '1' to '0') and at its end (nCS transitions from '0' to '1') is irrelevant.
- Fields D11-D0 (see Figure 9) contain the ADC conversion result.
- Fields AUX-CN2-CN1-CN0 by default contain the channel number for which the D11-D0 data was obtained.
- Fields B15-B0 contain the input part of the command.
- The output (response) part of the command, if provided, appears in fields D11-D4 (Section 6.6.5)
- The typical command length is 32 tSCLK, but it may be longer or shorter in different situations (see Section 6.6.8).

6.6.4 Device states

The following set of states is defined (see the diagram in Figure 10):

- **IDLE** – neutral state, no analog-to-digital conversion is performed;
- **INIT** – initialization of the internal registers of the device;
- **PROG** – not functionally required (for compatibility);
- **STDBY** – standby mode;
- **PWRDN** – software power-down mode;
- **MANCH** – analog-to-digital conversion with direct channel specification;
- **AUTO** – analog-to-digital conversion with automatic channel scanning based on the *Auto Sequence* mask (see Table 5);
- **AUTOR** – same as **AUTO**, but the minimum address from the *Auto Sequence* mask is selected;

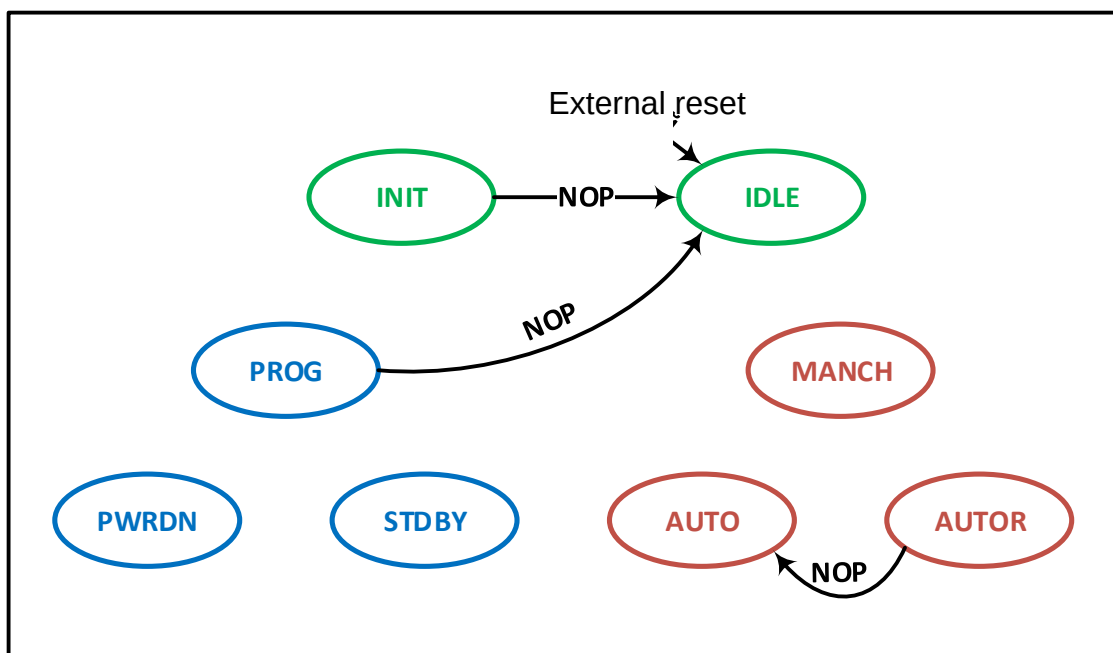


Figure 10 – State diagram and transitions between states

The chip state determines the actions performed in that state. The state transition rules are as follows:

- Transition to a new state is performed by the corresponding state command. For example, the **MANCH** command transitions the chip to the **MANCH** state regardless of the current state.
- The **NOP** command generally does not change the current state, with the following exceptions:
 - From the **AUTOR** state, a transition to the **AUTO** state occurs;
 - From the **INIT**, **PROG** states, a transition to the **IDLE** state occurs;
 - Any register read/write command behaves as a NOP with respect to state control.
- After reset or power-on, the device enters the **IDLE** state.
- A state change occurs at the end of a frame (on the rising edge of the nCS signal). The command contained in the frame is processed in the current (at the start of the frame) state of the device, and only after this processing is complete does the state change take effect.

The characteristics of the states and the permitted actions within them are as follows:

- in any state, a command to transition to any other state is permitted;
- analog-to-digital conversion is performed in the **MANCH**, **AUTO**, and **AUTOR** states;
- writing to internal registers is permitted in all states except **INIT**. In the **INIT** state, the registers are reset to their default values, so writing is meaningless;
- Reading of the internal registers via the SPI interface is possible in all states except **INIT**, **MANCH**, **AUTO**, **AUTOR**. In the **INIT** state, the registers are reset to their default state, so reading is meaningless. In the **MANCH**, **AUTO**, **AUTOR** output serial data line is busy transmitting the ADC conversion result, therefore transmission of the data of the readable registers is not possible;
- in any state, the chip transmits the following information from neighbors on the Daisy Chain:
 - in the **MANCH**, **AUTO**, **AUTOR** states – the ADC conversion result;
 - in other states – the data of the readable registers.

6.6.5 SPI commands

The available serial interface commands are listed in Table 4 and Table 5. The most significant 15 bits of the command (RW) determine whether it is a write ('1') or read ('0') operation on the internal registers. Fields 14-8 – address bits (A6-A0), fields 7-0 – data bits of the command (D7-D0).

The following command execution features must be considered:

- The data in the register being written is updated on the 16th falling edge of the SCLK signal, when the SPI command input data has been fully received on the SDI line.
- The data read from the register is output on the SDO line, starting from the 16th falling edge of the SCLK signal and continues for eight clock cycles (Figure 11).
- Both write and read operations to internal registers are performed within the state in which the SPI command is executed.
- Execution of state change commands, as mentioned in 6.6.4, is not synchronized with the SCLK signal and is performed on the rising edge of the nCS signal.

Table 4 – State change commands

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<u>RW</u>	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IDLE	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
INIT	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1
STDBY	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0
PWRDN	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1
PROG	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0
AUTOR	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1
AUTO	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
MANAUX	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
MANCH	1	1	1	1	1	1	1	1	1	1	1	1	1	Channel ¹		

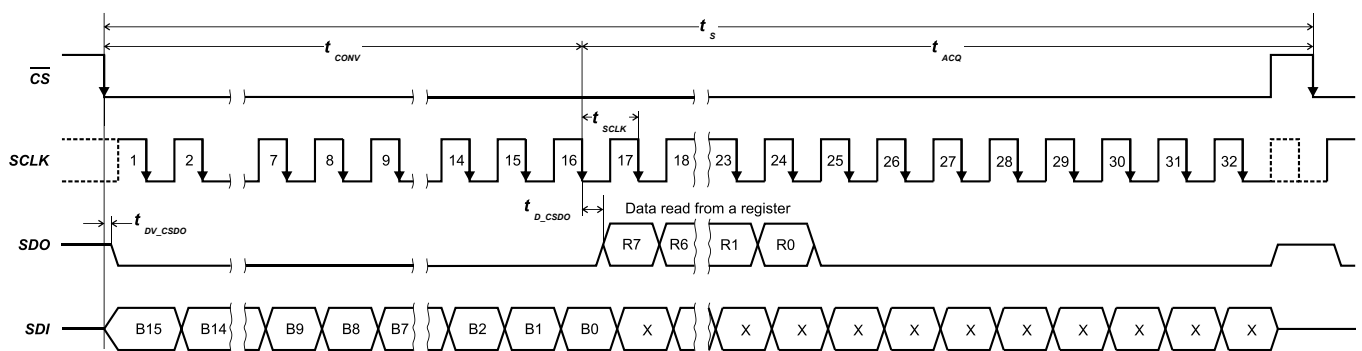


Figure 11 – Register read timing diagram over SPI

¹ Three-bit channel number, which will be digitized

Table 5 – Internal register read/write commands

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default	
	<u>R</u> W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
Channel Input Range	0/1	0	0	0	0	0	0	0	GAIN ¹			U ²	nD ³	Channel ⁴			0x08	
Auto Sequence	0/1	0	0	0	1	0	0	0	0	Channel Mask ⁵								0xFF
Channel Power Down	0/1	0	0	0	1	0	0	0	1	Channel Mask ⁶								0x00
Alarm Hysteresis	0/1	0	0	0	0	0	0	1	0	Hysteresis ⁶				Channel ⁵			0x00	
Alarm Overview Tripped-Flag	0	0	0	0	0	0	0	1	1	Channel Mask ⁷								0x00 ⁸
Alarm Tripped-Flag Low	0	0	0	0	0	0	1	0	0	Channel Mask ⁸								0x00 ⁹
Alarm Tripped-Flag High	0	0	0	0	0	0	1	0	1	Channel Mask ⁸								0x00 ⁹
Alarm Active-Flag Low	0	0	0	0	0	0	1	1	0	Channel Mask ⁸								0x00 ⁹
Alarm Active-Flag High	0	0	0	0	0	0	1	1	1	Channel Mask ⁸								0x00 ⁹
Alarm Threshold	0/1	0	0	0	0	1	Channel ⁵			H/L ⁹	M/L ¹⁰	Threshold ¹¹					0x3F / 00	
Feature	0/1	0	1	0	0	0	0	0	1	Daisy# ¹²		SE ¹³	AEN ¹⁴	AAF ¹⁵	-	SDO ¹⁶	0x00	

¹ PGA of Channel № (See Table 2)

² Bipolar («0») or unipolar («1») mode of the channel operation (See Table 2)

³ Differential («0») or single-ended («1») mode of the channel operation (See Table 2)

⁴ Three-bit channel number (0-7) for which a mode is set.

⁵ Eight-bit mask for the channels (the bit number corresponds to the channel number). Necessary channels must be designated to «1», others – «0»

⁶ Five-bit hysteresis of the Alarm feature

⁷ The state of the Alarm flag in each channel (the bit number corresponds to the channel number). Read only

⁸ While is not changed as a result of Alarm operation

⁹ Upper («1») / lower («0») value of Alarm threshold

¹⁰ Most significant («1») / least significant («0») part of the 12-bit threshold value of the Alarm

¹¹ The value of the Alarm threshold (a half of the word)

¹² IC's number for the identification in the Daisy Chain

¹³ The ADC operates in the single-ended («1») / differential («0») mode at the direct access to AUX

¹⁴ The Alarm function is enabled («1») / disabled («0»)

¹⁵ The ALARM input connects active («1») / latched («0») flags

¹⁶ Defines the information to be presented in AUX-CN2-CN1-CN0 fields of the frame (See Figure 9):
«00» - channel address; «01» - channel mode; «10» - Daisy#¹³; «11» - nothing

6.6.6 The Daisy Chain

The SPI IRL5111FI interface supports synchronous acquisition of output samples from multiple devices connected in a serial chain, as shown in Figure 12. The $\overline{nCS}$, SCLK and SDI – pins are common to all devices and are controlled by three microcontroller pins. The DAISY₁ pin of the first ADC in the chain is tied to logic "0", and its output SDO₁ – is connected to the DAISY₂ input of the second ADC, and so on. The SDO_N output of the last ADC in the chain is connected to the SDI input of the microcontroller.

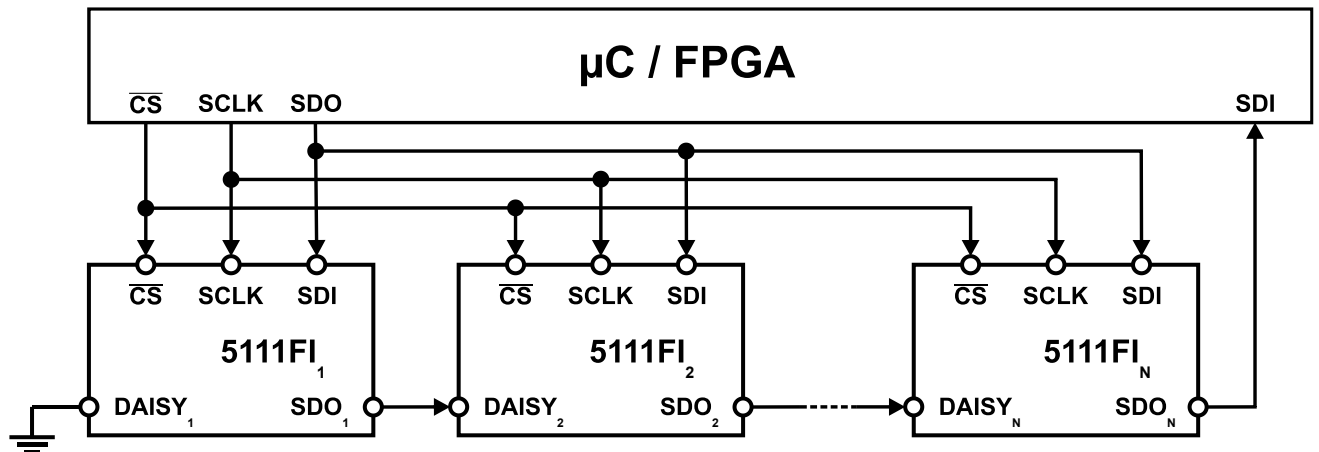


Figure 12 – Connecting multiple devices in a Daisy Chain

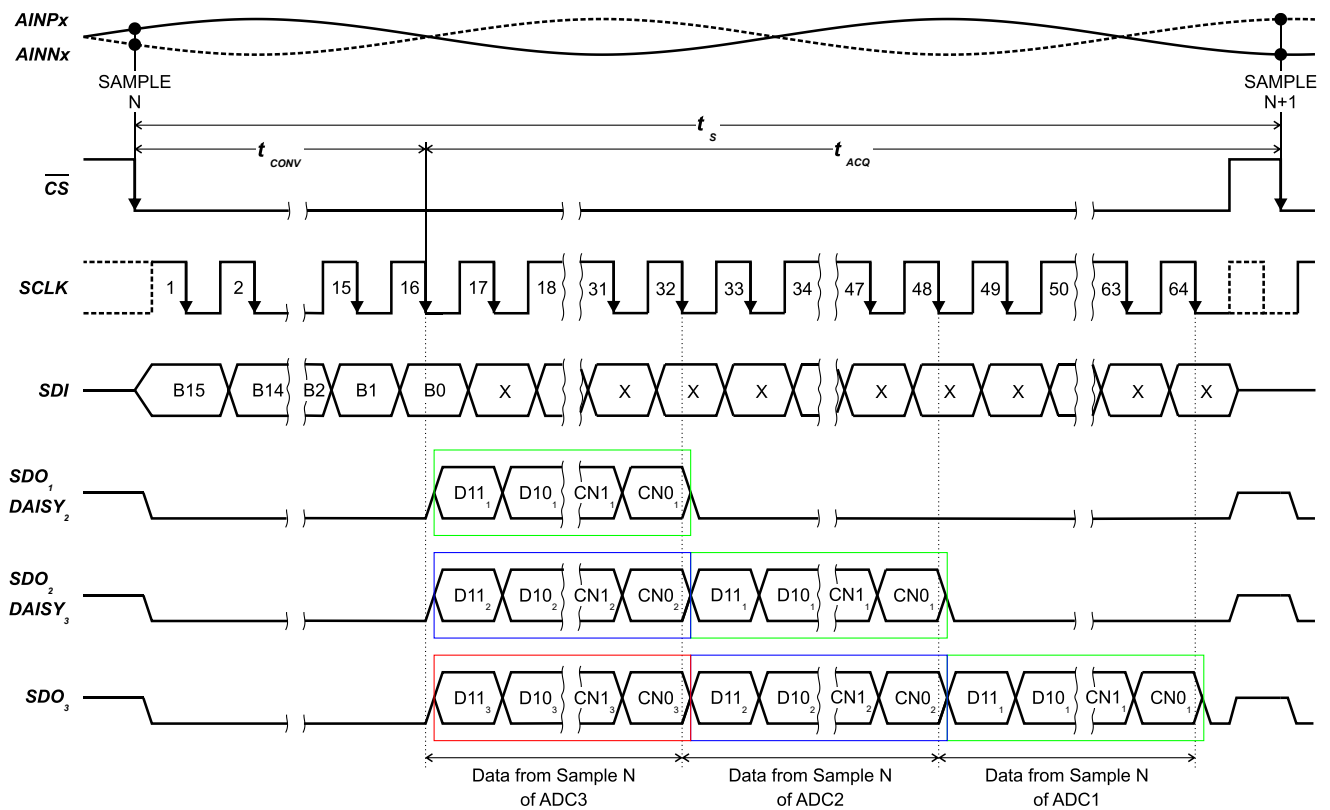


Figure 13 – Timing diagram of three devices in a Daisy Chain during analog-to-digital conversion

An example timing diagram for three devices connected in a Daisy Chain is shown in Figure 13. On the falling edge of $\overline{nCS}$ all three devices sample the signal from their channels and start analog-to-digital conversion. During the first 16 clock cycles of SCLK a command common to all three devices can be transmitted on the SDI. Starting from the 16th clock cycle, each ADC outputs the conversion result on its SDO pin and simultaneously shifts it into the shift register of the next device via its DAISY input. The contents of the shift register are output starting from the 33rd clock cycle and onwards. No special configuration is required for Daisy Chain operation – it is sufficient to only increase the packet length.

Thus, when IRL5111FI devices are connected according to the Figure 12 scheme, the digital controller first receives the conversion result of ADC N, then ADC N-1 and so on, with the output of each result starting from the most significant bit. In the example of Figure 13, $3 \cdot 16 = 48$ clock cycles of SCLK are required to capture the results of all three ADCs in the chain, plus an additional 16 clock cycles at the beginning for the input command. Therefore, the total packet length must be increased to 64 clock cycles. This extension of the SPI packet results in the overall system throughput decreasing proportionally to the number of devices connected in the chain.

When using the Daisy Chain topology, the following must also be considered:

- Reading registers takes 8 clock cycles instead of 16, so propagating the read data through the Daisy Chain takes less time: for three devices – 40 clock cycles (Figure 14).
- Since the SDI inputs of all devices in the chain are connected together, in the general case they all operate with identical settings. This limitation can be bypassed by complicating the system control, assigning the controller individual control of the $\overline{nCS}$ or SDI pins.
- As the number of devices in the chain increases, the load on the shared SPI lines ($\overline{nCS}$, SDI, SDO) increases, which may lead to violations of the requirements for signal edges and delays in the timing diagram Figure 9. Using additional digital buffers on the shared lines will help solve this problem in most cases.

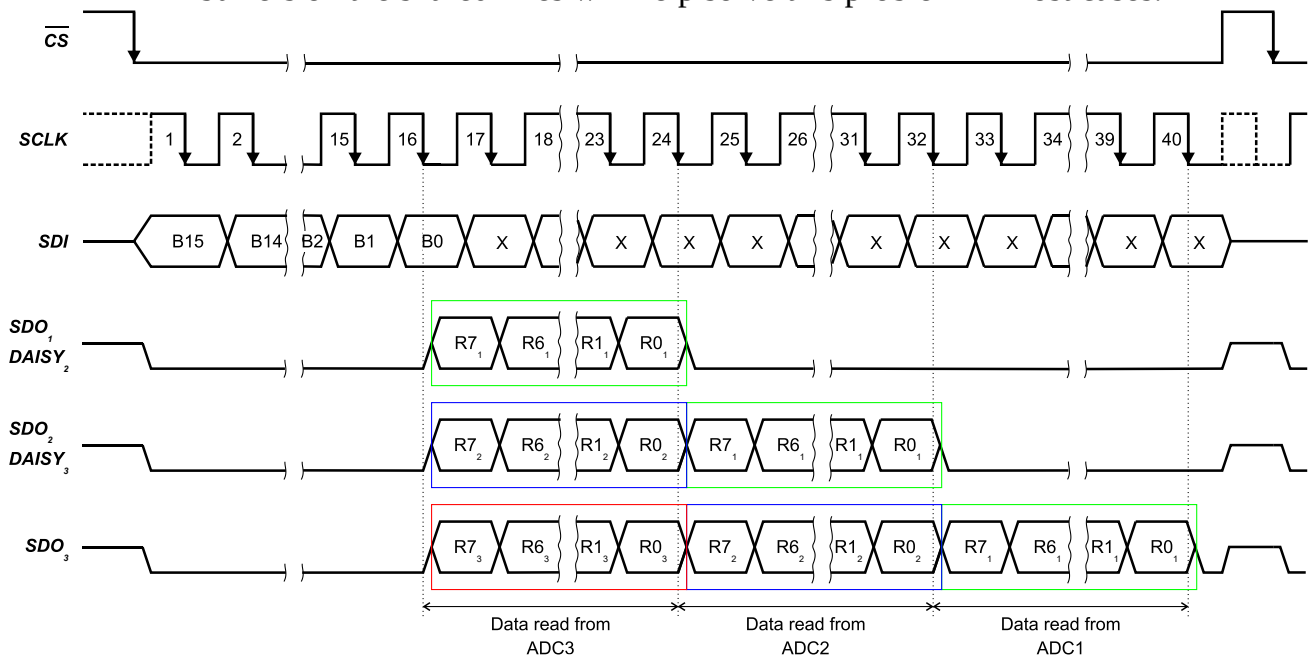


Figure 14 – Timing diagram of three devices in a Daisy Chain when reading internal registers

6.6.7 The Alarm feature

The device implements an input analog signal monitoring function, which allows for a rapid response to its excursion beyond the predefined threshold values. The corresponding flag registers, as well as the signal on the ALARM pin, are updated on the 16th falling edge of the SCLK signal in states that perform analog-to-digital conversion (MANCH, AUTO, AUTOR), and do not change between conversions.

To define the threshold conditions for Alarm triggering, each channel has (see Table 5):

- 12-bit lower and upper threshold registers. Information is written to these registers using the SPI Alarm Threshold command. The fields of this command define:
 - *Channel* – channel number;
 - *H/L* – upper or lower threshold;
 - *M/L* – upper or lower six bits of the 12-bit threshold;
 - *Threshold* – the value of the 6-bit half of the 12-bit threshold code.

To define two 12-bit thresholds in a single channel, four SPI commands *Alarm Threshold* are required. By-default, the upper thresholds contain all “1”, and the lower ones – all “0”.

- 5-bit hysteresis register. Writing information to this register is performed using the SPI command *Alarm Hysteresis*. The fields of this command define:
 - *Channel* – channel number;
 - *Hysteresis* – the value of the 5-bit hysteresis code.

By-default, all hysteresis values are equal to zero.

For each channel, active high and low threshold flags are defined.

The high threshold flag (Alarm Flag High) is set to “1” when the conversion result of this channel exceeds the high threshold T by the hysteresis value H , and is reset when the output code becomes less than or equal to T .

Similarly, the low threshold flag (*Alarm Flag Low*) is set when the digital output of this channel drops below the low threshold adjusted for hysteresis $T-H$ and is reset to “0” when the digital output is greater than or equal to T .

These flag activation rules for crossing the high and low thresholds are shown in Figure 15 – Activation of Alarm flags upon crossing the high and low thresholds¹⁵. Adding and subtracting the threshold and hysteresis is performed with clamping to the minimum and maximum value for a 12-bit code.

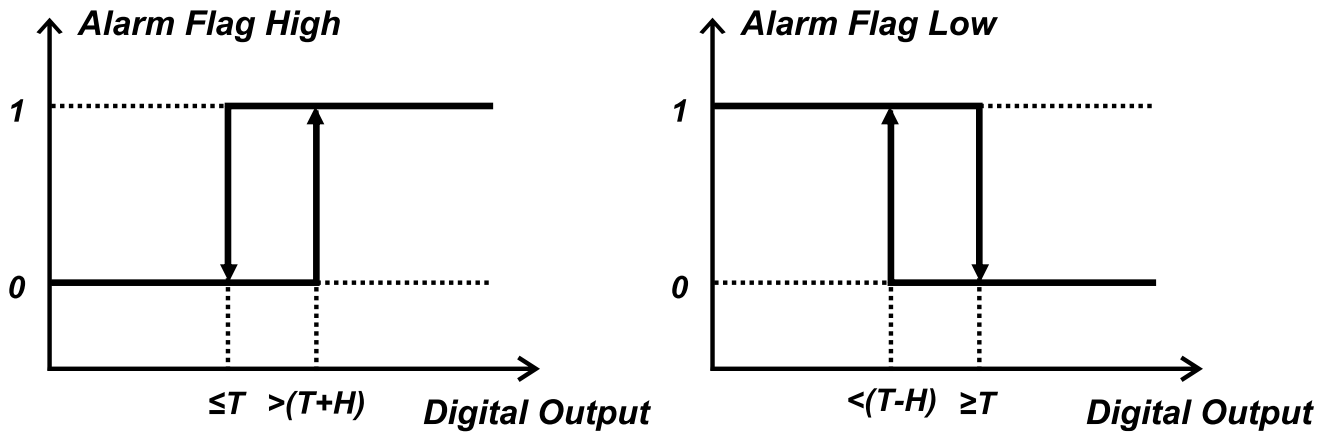


Figure 15 – Activation of Alarm flags upon crossing the high and low thresholds¹⁵

In addition to the active flags (*Alarm-Active Flag*), latched flags (*Alarm-Tripped Flag*) for the high and low thresholds are provided for each channel. The latched flag is set in the same way as the active flag, but is reset only by reading the flag register. Since reading registers is not possible without interrupting the analog-to-digital conversion (see Section 6.6.4), latched flags, which retain information about threshold exceedance events, allow for less frequent register reads and, consequently, less frequent interruption of the conversion.

To read the state of the flag registers of Alarm, the following commands are provided (see Table 5):

- *Alarm Active-Flag Low* – active flags lower threshold crossing;
- *Alarm Active-Flag High* – active flags crossing of the upper threshold;
- *Alarm Tripped-Flag Low* – latched flags lower threshold crossing (cleared after read);
- *Alarm Tripped-Flag High* – latched flags crossing of the upper threshold (cleared after read);
- *Alarm Overview Tripped-Flag* – latched flags upper and lower, combined with OR (not cleared after read).

Each of these commands returns an 8-bit word in which bit i contains the state of the flag for channel i .

In addition to reading flag registers via the SPI interface, indication of the overall result of the Alarm function is provided on the ALARM pin of the device. A high level on the ALARM signal indicates that the conversion result has exceeded the set upper or lower threshold in at least one channel.

A typical use case for the ALARM pin is generating an interrupt signal for an external controller. Upon receiving this interrupt, the controller can read the Alarm flag registers and determine the channel (or channels) in which the input signal exceeded the specified range.

When the AAF field = “1”, the Feature register (see Table 5) outputs the logical OR of the active flags (upper and lower, across all channels) to the ALARM pin. If AAF = “0”, the logical OR of the latched flags (also upper and lower, across all channels) is output to the ALARM pin.

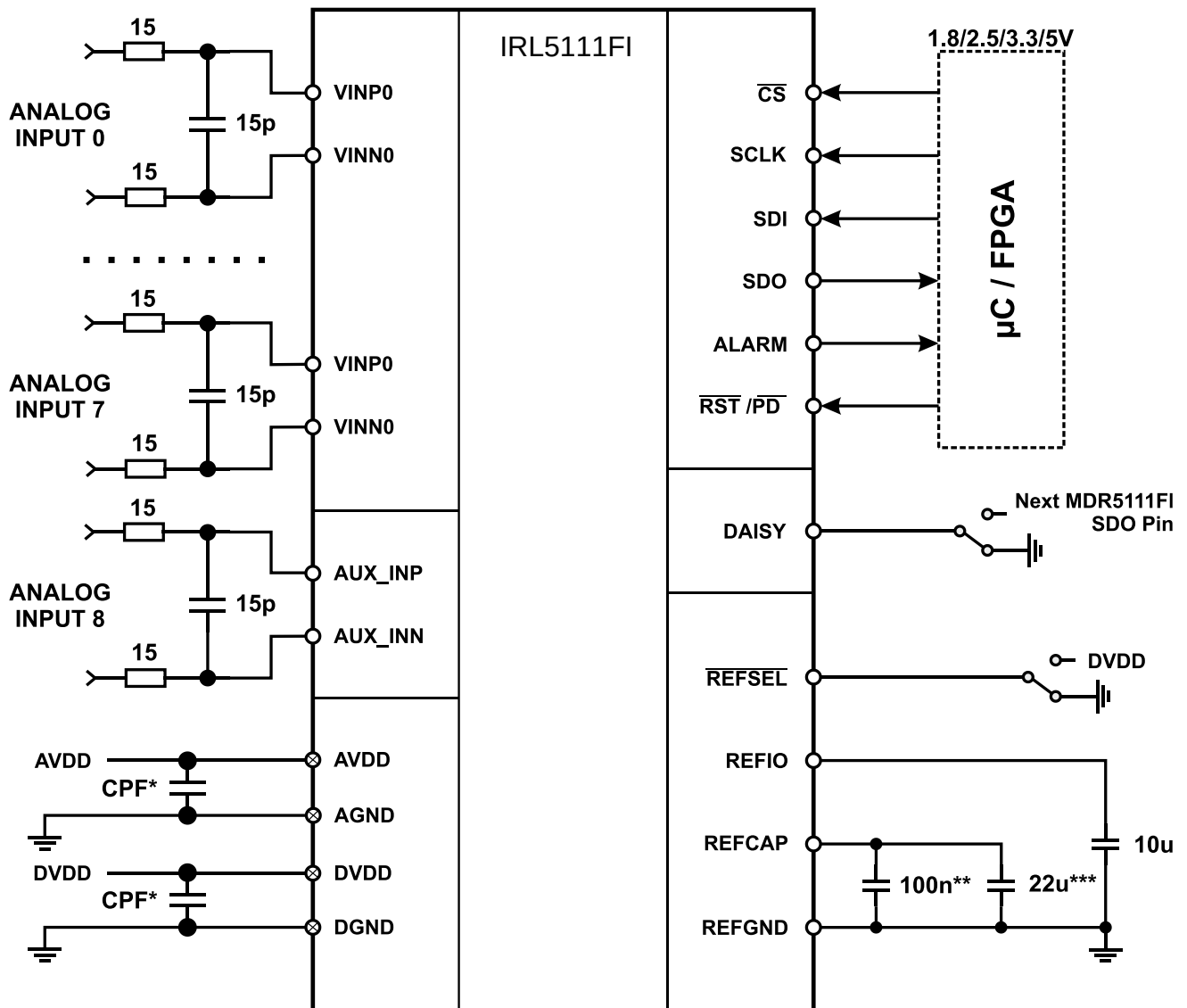
To access the functionality described in this section, it is necessary to enable the Alarm function by writing “1” to the AEN field of the Feature register.

6.6.8 Non-standard SPI message length

The typical length of an SPI message is 32 SCLK clock cycles SCLK. 16 clock cycles are required for the command input data and 16 for the conversion result output. In some cases, other command durations are allowed for SPI:

- For commands that change states or write to mode registers, 16 SCLK cycles are sufficient.
- For commands that read mode registers, 24 SCLK cycles are sufficient: 16 cycles for the command input data and 8 cycles for the register data.
- If not all bits of the analog-to-digital conversion result are important for the application, the command can be shortened. For example, 26 SCLK cycles are sufficient to transmit 10 bits.
- Transmitting data to neighbors in the Daisy Chain requires additional SCLK cycles (see Section 6.6.6).
- If the message contains fewer than 16 SCLK cycles, no actions (register or state changes) are performed.
- If the message contains more than 16 SCLK periods but fewer than required for a complete data transfer, the register or state change is performed, but part of the output data is lost.
- To stabilize the signal at the ADC input during sampling, a minimum specified sampling time is required from the 16th falling edge of the SCLK signal of the current SPI message to the falling edge of the nCS signal of the next message (see Section 6.6.1). This time must be accounted for when formatting the SPI operation.

7 Typical connection diagram



Notes:

* Filter Capacitors: 10 uF + ceramic 100 nF at each power pin

** Ceramic low ESR capacitor

*** ESR < 1.5 Ohm

Figure 16 – Typical connection diagram

8 Electrical characteristics of the device

Table 6 – Electrical characteristics of the device at incoming inspection and shipment

Parameter Name, unit of measurement, measurement mode	Parameter letter designation	Limit parameter		Ambient temperature, °C
		not less than	not more than	
High-level output voltage, V,	U_{OH}	$0,8 \cdot U_{CC}$	U_{CC}	25, 85, – 40
Low-level output voltage, V,	U_{OL}	0	$0,2 \cdot U_{CC}$	25, 85, – 40
High-level leakage current, μA , at digital input	I_{ILH}	–	5,0	25, 85, – 40
Low-level leakage current, μA , at digital input	I_{ILL}	– 5,0	–	25, 85, – 40
High-level output current in "Off" state, μA ,	I_{OZH}	–	5,0	25, 85, – 40
Low-level output current in the "Off" state, μA	I_{OZL}	– 5,0	–	25, 85, – 40
Dynamic supply current, mA, at DVDD	I_{CCO}	–	1,0	25, 85, – 40
Dynamic supply current, mA, on the AVDD	I_{CCOA}	–	20	25, 85, – 40
Power consumption in Off mode, mA, on the DVDD	I_{CCZ}	–	10	25, 85, – 40
Power consumption in Off mode, mA, on the AVDD	I_{CCZA}	–	60	25, 85, – 40
Signal-to-noise ratio, dB, at an input signal frequency of 1 kHz	SNR	67	–	25, 85, – 40
Harmonic-free range, dB, at an input signal frequency of 1 kHz	SFDR	72	–	25, 85, – 40

9 Absolute maximum ratings of the integrated circuit

Table 7 – Absolute maximum and operating limits of the integrated circuits

Parameter name, unit of measurement	Alphanumeric Parameter symbol	Absolute Maximum Ratings		Absolute maximum	
		not less than	not more than	not less than	not more than
Analog block supply voltage, V	U_{CCA}	4,75	5,25	-0,3	6,0
Digital interface supply voltage, V,	U_{CC}	1,62	$U_{CCA}^{1)}$	-0,3	6,0
High-level input voltage, V, at digital inputs: – when $U_{CC} > 2.1$ V; – when $U_{CC} \leq 2.1$ V	U_{IH}	$0,7 \cdot U_{CC}$	U_{CC}	–	$U_{CC} + 0,3$
		$0,8 \cdot U_{CC}$			
Input low level voltage, V, on digital inputs: – when $U_{CC} > 2.1$ V; – when $U_{CC} \leq 2.1$ V	U_{IL}	0	$0,3 \cdot U_{CC}$	-0,3	–
			$0,2 \cdot U_{CC}$		
Input voltage, V, on the analog inputs AUX_INP, AUX_INN	U_{IA}	0	U_{REF}	-0,3	$U_{CC} + 0,3$
Input voltage, V, on the analog inputs AINP0, AINP1, ... AINP7: – range $\pm 2.5 \cdot U_{REF}^{2)}$ single-wire;	U_{IAP}	$-2,5 \cdot U_{REF}$	$2,5 \cdot U_{REF}$	-20	20
– range $\pm 1.25 \cdot U_{REF}$ single-wire;		$-1,25 \cdot U_{REF}$	$1,25 \cdot U_{REF}$		
– range $\pm 0.625 \cdot U_{REF}$ single-wire;		$-0,625 \cdot U_{REF}$	$0,625 \cdot U_{REF}$		
– range $\pm 0.3125 \cdot U_{REF}$ single-wire;		$-0,3125 \cdot U_{REF}$	$0,3125 \cdot U_{REF}$		
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;		$-0,15625 \cdot U_{REF}$	$0,15625 \cdot U_{REF}$		
– range $2.5 \cdot U_{REF}$ single-wire;		0	$2,5 \cdot U_{REF}$		
– range $1.25 \cdot U_{REF}$ single-ended;		0	$1,25 \cdot U_{REF}$		
– range $0.625 \cdot U_{REF}$ single-ended;		0	$0,625 \cdot U_{REF}$		
– range $0.3125 \cdot U_{REF}$ single-ended;		0	$0,3125 \cdot U_{REF}$		
– range $\pm 1.25 \cdot U_{REF}$ differential;		$-1,25 \cdot U_{REF}$	$1,25 \cdot U_{REF}$		

Parameter name, unit of measurement	Alphanumeric Parameter symbol	Absolute Maximum Ratings		Absolute maximum	
		not less than	not more than	not less than	not more than
– range $\pm 0.625 \cdot U_{REF}$ differential;		$-0,625 \cdot U_{REF}$	$0,625 \cdot U_{REF}$		
– range $\pm 0.3125 \cdot U_{REF}$ differential;		$-0,3125 \cdot U_{REF}$	$0,3125 \cdot U_{REF}$		
– range $\pm 0.15625 \cdot U_{REF}$ differential;		$-0,15625 \cdot U_{REF}$	$0,15625 \cdot U_{REF}$		
– range $\pm 0.078125 \cdot U_{REF}$ differential;		$-0,078125 \cdot U_{REF}$	$0,078125 \cdot U_{REF}$		
– range $2.5 \cdot U_{REF}$ differential;		0	$2,5 \cdot U_{REF}$		
– range $1.25 \cdot U_{REF}$ differential;		0	$1,25 \cdot U_{REF}$		
– range $0.625 \cdot U_{REF}$ differential;		0	$0,625 \cdot U_{REF}$		
– range $0.3125 \cdot U_{REF}$ differential;		0	$0,3125 \cdot U_{REF}$		
– range $0.15625 \cdot U_{REF}$ differential;		0	$0,15625 \cdot U_{REF}$		
Input voltage, V, on analog inputs AINN0, AINN1, ... AINN7:	U_{IAN}			-20	20
– range $\pm 2.5 \cdot U_{REF}^{(2)}$ single-ended;		-0,1	0,1		
– range $\pm 1.25 \cdot U_{REF}$ single- ended;		-0,1	0,1		
– range $\pm 0.625 \cdot U_{REF}$ single- wire;		-0,1	0,1		
– range $\pm 0.3125 \cdot U_{REF}$ single- wire;		-0,1	0,1		
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;		-0,1	0,1		
– range $2.5 \cdot U_{REF}$ single-wire;		-0,1	0,1		
– range $1.25 \cdot U_{REF}$ single- wire;		-0,1	0,1		
– range $0.625 \cdot U_{REF}$ single- wire;		-0,1	0,1		
– range $0.3125 \cdot U_{REF}$ single- ended;		-0,1	0,1		
– range $\pm 1.25 \cdot U_{REF}$ differential;		$-1,25 \cdot U_{REF}$	$1,25 \cdot U_{REF}$		
– range $\pm 0.625 \cdot U_{REF}$ differential;		$-0,625 \cdot U_{REF}$	$0,625 \cdot U_{REF}$		

Parameter name, unit of measurement	Alphanumeric Parameter symbol	Absolute Maximum Ratings		Absolute maximum	
		not less than	not more than	not less than	not more than
– range $\pm 0.3125 \cdot U_{REF}$ differential;		-0,3125· U_{REF}	0,3125· U_{REF}		
– range $\pm 0.15625 \cdot U_{REF}$ differential;		-0,15625· U_{REF}	0,15625· U_{REF}		
– range $\pm 0.078125 \cdot U_{REF}$ differential;		-0,078125· U_{REF}	0,078125· U_{REF}		
– range $2.5 \cdot U_{REF}$ differential;		0	2,5· U_{REF}		
– range $1.25 \cdot U_{REF}$ differential;		0	1,25· U_{REF}		
– range $0.625 \cdot U_{REF}$ differential;		0	0,625· U_{REF}		
– range $0.3125 \cdot U_{REF}$ differential;		0	0,3125· U_{REF}		
– range $0.15625 \cdot U_{REF}$ differential;		0	0,15625· U_{REF}		
External reference voltage on the REFIO pin, V	U_{REFIO}	4,0	4,2	-0,3	$U_{CC} + 0,3$
Output current on the REFIO pin, μA	I_{REFIO}	–	2	–	20
Current on the REFCAP pin, μA	I_{REFCAP}	-10	10	-20	20
High-level output current, mA	I_{OH}	–	0,5	–	1,0
Low-level output current, mA	I_{OL}	-0,5	–	-1,0	–
Sampling frequency, MS/s	f_S	–	0,5	–	–
Full conversion period, μs	t_S	2	–	–	–
Duration of the sample phase of the input signal, ns	t_{ACQ}	1088	–	–	–
Successive approximation algorithm execution time, ns	t_{CONV}	912	–	–	–
Serial interface clock signal pulse frequency, MHz	f_{SCLK}	–	17	–	–
Serial interface clock signal period, ns	t_{SCLK}	58,8	–	–	–
Time between the falling edge of nCS and the falling edge of SCLK, ns	t_{SU_CSCK}	30	–	–	–
High-level duration of nCS, ns	t_{PH_CS}	30	–	–	–
High-level duration of SCLK, fraction of $t_{SCLK}^{3)}$	t_{PH_CK}	0,4	0,6	–	–

Parameter name, unit of measurement	Alphanumeric Parameter symbol	Absolute Maximum Ratings		Absolute maximum	
		not less than	not more than	not less than	not more than
Delay between the last falling edge of the frame and the rising edge of SCLK and the rising edge of nCS, ns	t_{D_CSCK}	10	—	—	—
Data setup time on the SDI pin with respect to the falling edge of SCLK, ns	t_{SU_DICK}	5	—	—	—
Data hold time on the SDI pin with respect to the falling edge of SCLK, ns	t_{HT_CKDI}	5	—	—	—
Digital pin load capacitance, pF	C_L	—	20	—	—
Output resistance of the input analog signal source, k Ω	R_S	—	20	—	—
1) 3.3 V at incoming inspection; 2) $U_{REF} = U_{REFI}$ in internal voltage reference mode, $U_{REF} = U_{REFO}$ in external voltage reference mode 3) $t_{SCLK} = 1 / f_{SCLK}$ Note – Simultaneous application of two or more absolute maximum ratings is not permitted					

10 Reference data

Table 8 – Chip reference parameters

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
Input impedance at analog inputs AINP0, AINN0,... AINP7, AINN7, MΩ:	R_{IN}	0,85	1,16	2,0	25, 85, – 40
– range $\pm 2.5 \cdot U_{REF}$ single-ended;			1,24		
– range $\pm 1.25 \cdot U_{REF}$ single-ended;			1,38		
– range $\pm 0.625 \cdot U_{REF}$ single-ended;			1,56		
– range $\pm 0.3125 \cdot U_{REF}$ single-wire;			1,74		
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;			1,24		
– range $2.5 \cdot U_{REF}$ single-wire;			1,37		
– range $1.25 \cdot U_{REF}$ single-wire;			1,54		
– range $0.625 \cdot U_{REF}$ single-wire;			1,74		
– range $0.3125 \cdot U_{REF}$ single-wire;			1,16		
– range $\pm 1.25 \cdot U_{REF}$ differential;			1,24		
– range $\pm 0.625 \cdot U_{REF}$ differential;			1,38		
– range $\pm 0.3125 \cdot U_{REF}$ differential;			1,56		
– range $\pm 0.15625 \cdot U_{REF}$ differential;			1,74		
– range $\pm 0.078125 \cdot U_{REF}$ differential;			1,16		
– range $2.5 \cdot U_{REF}$ differential;			1,24		
– range $1.25 \cdot U_{REF}$ differential;			1,38		
– range $0.625 \cdot U_{REF}$ differential;			1,56		
– range $0.3125 \cdot U_{REF}$ differential;			1,74		
– range $0.15625 \cdot U_{REF}$ differential;					
Input current at analog inputs AINP0, AINN0,... AINP7, AINN7, A:	I_{IN}		$\frac{U_{INA} - 2,26}{R_{IN}}$		25, 85, – 40
– range $\pm 2.5 \cdot U_{REF}$ single-ended;			$\frac{U_{INA} - 2,08}{R_{IN}}$		
– range $\pm 1.25 \cdot U_{REF}$ single-wire;			$\frac{U_{INA} - 1,78}{R_{IN}}$		
– range $\pm 0.625 \cdot U_{REF}$ single-wire;			$\frac{U_{INA} - 1,39}{R_{IN}}$		
– range $\pm 0.3125 \cdot U_{REF}$ single-wire;					

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;			$\frac{U_{INA} - 0,96}{R_{IN}}$		
– range $2.5 \cdot U_{REF}$ single-wire;			$\frac{U_{INA} - 2,07}{R_{IN}}$		
– range $1.25 \cdot U_{REF}$ single-wire;			$\frac{U_{INA} - 1,77}{R_{IN}}$		
– range $0.625 \cdot U_{REF}$ single-ended;			$\frac{U_{INA} - 1,38}{R_{IN}}$		
– range $0.3125 \cdot U_{REF}$ single-ended;			$\frac{U_{INA} - 0,96}{R_{IN}}$		
– range $\pm 1.25 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 2,26}{R_{IN}}$		
– range $\pm 0.625 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 2,08}{R_{IN}}$		
– range $\pm 0.3125 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 1,78}{R_{IN}}$		
– range $\pm 0.15625 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 1,39}{R_{IN}}$		
– range $\pm 0.078125 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 0,96}{R_{IN}}$		
– range $2.5 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 2,26}{R_{IN}}$		
– range $1.25 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 2,08}{R_{IN}}$		
– range $0.625 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 1,78}{R_{IN}}$		
– range $0.3125 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 1,39}{R_{IN}}$		
– range $0.15625 \cdot U_{REF}$ differential;			$\frac{U_{INA} - 0,96}{R_{IN}}$		
Overvoltage protection on analog inputs AINP0, AINN0,... AINP7, AINN7, V	U_{OVP}	-20		20	25, 85, – 40
Differential nonlinearity, LSB	DNL	-0,5	$\pm 0,2$	0,5	25, 85, – 40
Integral nonlinearity, LSB: – range $\pm 2.5 \cdot U_{REF}$ single-ended;	INL	-1,5	± 1	1,5	25, 85, – 40
– range $\pm 1.25 \cdot U_{REF}$ single-ended;			$\pm 0,75$		
– range $\pm 0.625 \cdot U_{REF}$ single-ended;			$\pm 0,65$		
– range $\pm 0.3125 \cdot U_{REF}$ single-wire;			$\pm 0,6$		
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;			$\pm 0,55$		
– range $2.5 \cdot U_{REF}$ single-wire;			$\pm 0,75$		
– range $1.25 \cdot U_{REF}$ single-wire;			$\pm 0,65$		

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
– range $0.625 \cdot U_{REF}$ single-wire;			$\pm 0,6$		
– range $0.3125 \cdot U_{REF}$ single-wire;			$\pm 0,55$		
– range $\pm 1.25 \cdot U_{REF}$ differential;			$\pm 0,6$		
– range $\pm 0.625 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $\pm 0.3125 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $\pm 0.15625 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $\pm 0.078125 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $2.5 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $1.25 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $0.625 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $0.3125 \cdot U_{REF}$ differential;			$\pm 0,55$		
– range $0.15625 \cdot U_{REF}$ differential;			$\pm 0,55$		
Gain error ³⁾ , %FS	E_{GE}		$\pm 0,05$		25
Temperature drift of gain error, PPM	$\Delta E_{GE} T$	-2		2	25, 85, – 40
Offset error, E_{MP}	E_{IO}		± 1		25
Temperature drift of offset error, E_{MP}	$\Delta E_{IO} T$	-2		2	25, 85, – 40
Signal-to-noise ratio, dB:	SNR		72,5		25, 85, – 40
– range $\pm 2.5 \cdot U_{REF}$ single-ended;			72,5		
– range $\pm 1.25 \cdot U_{REF}$ single-ended;			72,5		
– range $\pm 0.625 \cdot U_{REF}$ single-ended;			72,5		
– range $\pm 0.3125 \cdot U_{REF}$ single-wire;			72,3		
– range $\pm 0.15625 \cdot U_{REF}$ single-wire;			71,8		
– range $2.5 \cdot U_{REF}$ single-wire;			72,5		
– range $1.25 \cdot U_{REF}$ single-wire;		70,1	72,4		
– range $0.625 \cdot U_{REF}$ single-wire;		70,1	72,3		
– range $0.3125 \cdot U_{REF}$ single-wire;		70,1	71,7		

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
– range $\pm 1.25 \cdot U_{REF}$ differential;		70,1	72,5		
– range $\pm 0.625 \cdot U_{REF}$ differential;		70,1	72,5		
– range $\pm 0.3125 \cdot U_{REF}$ differential;		70,1	72,5		
– range $\pm 0.15625 \cdot U_{REF}$ differential;		70,1	72,4		
– range $\pm 0.078125 \cdot U_{REF}$ differential;		70,1	72,0		
– range $2.5 \cdot U_{REF}$ differential;		70,1	72,5		
– range $1.25 \cdot U_{REF}$ differential;		70,1	72,5		
– range $0.625 \cdot U_{REF}$ differential;		70,1	72,5		
– range $0.3125 \cdot U_{REF}$ differential;		70,1	72,4		
– range $0.15625 \cdot U_{REF}$ differential;		70,1	72,2		
Signal-to-noise ratio + distortion, dB	SNDR		71,2		25, 85, – 40
Total harmonic distortion, dB	THD		-78		25, 85, – 40
Harmonic-free range, dB:	SFDR	72	77		25, 85, – 40
– range $\pm 2.5 \cdot U_{REF}$ single-ended;		74	80		
– range $\pm 1.25 \cdot U_{REF}$ single-ended;		74	80		
– range $\pm 0.625 \cdot U_{REF}$ single-ended;		74	80		
– range $\pm 0.3125 \cdot U_{REF}$ single-ended;		74	80		
– range $\pm 0.15625 \cdot U_{REF}$ single-ended;		74	81		
– range $2.5 \cdot U_{REF}$ single-ended;		74	80		
– range $1.25 \cdot U_{REF}$ single-ended;		74	81		
– range $0.625 \cdot U_{REF}$ single-ended;		74	81		
– range $0.3125 \cdot U_{REF}$ single-ended;		74	81		
– range $\pm 1.25 \cdot U_{REF}$ differential;		74	80		
– range $\pm 0.625 \cdot U_{REF}$ differential;		74	80		
– range $\pm 0.3125 \cdot U_{REF}$ differential;		74	80		
– range $\pm 0.15625 \cdot U_{REF}$ differential;		74	80		

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
– range $\pm 0.078125 \cdot U_{REF}$ differential;		74	81		
– range $2.5 \cdot U_{REF}$ differential;		74	81		
– range $1.25 \cdot U_{REF}$ differential;		74	81		
– range $0.625 \cdot U_{REF}$ differential;		74	81		
– range $0.3125 \cdot U_{REF}$ differential;		74	80		
– range $0.15625 \cdot U_{REF}$ differential;		74	81		
Small-signal bandwidth at -3 dB, kHz	BW ₋₃	11,5	14,3	20,0	25, 85, – 40
Small-signal bandwidth at -0.1 dB, kHz	BW _{-0,1}	3,8	5,2	5,4	25, 85, – 40
Input capacitance on AUX_INP, AUX_INN, pF, in direct ADC access mode:	C _I		15		25
– during sampling			5		
– during conversion					
Integral nonlinearity, LSB, in direct access mode to the ADC	INL _{AUX}	-1,5	± 1	1,5	25, 85, – 40
Differential nonlinearity, LSB, in direct access mode to the ADC	DNL _{AUX}	-0,75	$\pm 0,5$	0,75	25, 85, – 40
Gain error, %FS, in direct access mode to the ADC	E _{GE_AUX}		$\pm 0,1$		25, 85, – 40
Offset error, LSB, in direct access mode to the ADC	E _{IO_AUX}		± 1		25, 85, – 40
Signal-to-noise ratio, dB, in direct access mode to the ADC	SNR _{AUX}		72,4		25, 85, – 40
Signal-to-noise + distortion ratio, dB, in direct ADC access mode	SNDR _{AUX}		71,7		25, 85, – 40
Total harmonic distortion, dB, in direct ADC access mode	THD _{AUX}		-80		25, 85, – 40

Parameter name, unit of measurement, test conditions	Alphanumeric Parameter symbol	Parameter specification			Ambient temperature,
		not less than	typical	not more than	
Harmonic-free range, dB, in direct ADC access mode	SFDR _{AUX}	74	81		25, 85, – 40
Voltage at the REFIO pin, V, in internal reference voltage mode	U _{REFI}	4,094	4,096	4,098	25
Temperature drift ⁴⁾ of the voltage at the REFIO pin, ppm/°C, in internal reference voltage mode	$\Delta U_{REFI} T$		10	30	25, 85, – 40
ADC reference voltage at the REFCAP pin, V	U _{REFP}	4,094	4,096	4,098	25
Dynamic supply current on the AVDD pins: – normal mode, all channels enabled, sinusoidal signal processing, mA – normal mode, all channels enabled, static signal processing, mA – standby mode, mA – software shutdown mode, μ A – hardware off mode, μ A	I _{CCOA}	8	11	14	25, 85, – 40
	I _{CCOA_STC}		10,7		
	I _{CCOA_STDBY}		0,5		
	I _{CCZA_P}		3	51	
	I _{CCZA_A}		0,67	46	
Dynamic supply current, mA, on the DVDD	I _{CCO}		0,3		25, 85, – 40
Delay of the SDO pin transition to active state relative to the falling edge of nCS, ns	t _{DV_CSDO}		10		25
Data delay on the SDO pin relative to the falling edge of nCS, ns	t _{D_CSDO}		10		25
Delay of the SDO pin transition to tri-state relative to the rising edge of nCS, ns	t _{DZ_CSDO}		10		25
¹⁾ U_I – amplitude of the differential input signal voltage. ²⁾ f_I – frequency of the input sinusoidal signal at the analog inputs AINPx, AINNx ³⁾ With respect to the nominal U_{REFI} = 4.096 V (the gain error already accounts for the deviation of U_{REFI}). ⁴⁾ Calculated using the formula $10^6 \cdot \max(U_{REFI}[T]) - \min(U_{REFI}[T]) / U_{REFI}[T=25^{\circ}\text{C}] / (T_{\max} - T_{\min})$ Note – Parameter measurement mode, unless otherwise specified: U_{CC}=3.3V, U_{CCA}=5.0V, U_I=-0.5dBFS, f_I = 1kHz, R_S = 50 Ω, maximum sampling frequency, internal voltage reference 4.096V, C_L = 20 pF. Typical value at 25°C, minimum and maximum over the temperature range, for all input ranges					

11 Typical characteristics

Parameter measurement mode, unless otherwise specified: $U_{CC} = 3.3\text{ V}$, $U_{CCA} = 5.0\text{ V}$, $U_I = -0.5\text{ dBFS}$, $f_I = 1\text{ kHz}$, $R_S = 50\ \Omega$, maximum sampling frequency, internal voltage reference 4.096 V , $C_L = 20\text{ pF}$, temperature plus $25\text{ }^\circ\text{C}$.

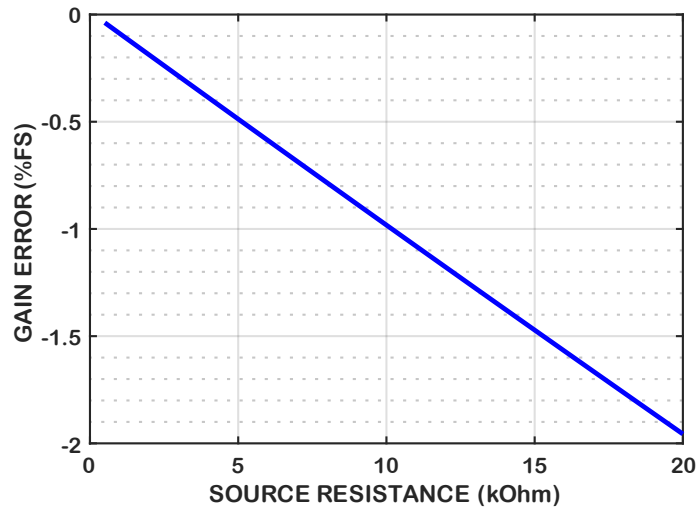


Figure 17 – Gain error versus output impedance of the analog signal source (for any range)

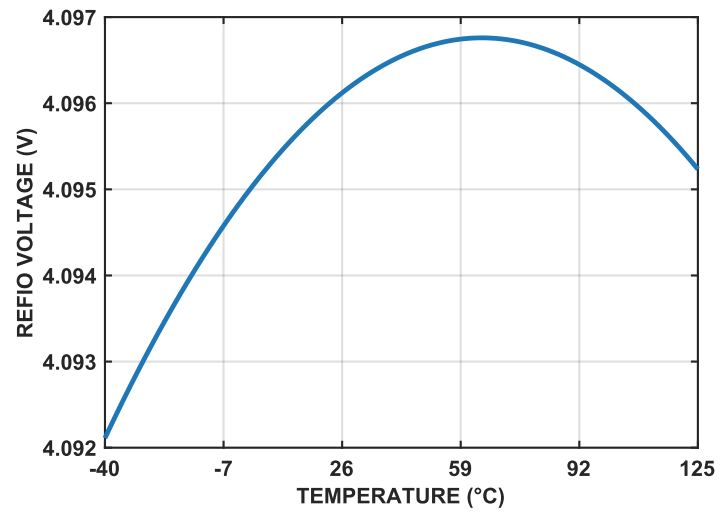


Figure 18 – Temperature dependence of the internal voltage reference output (REFIO)

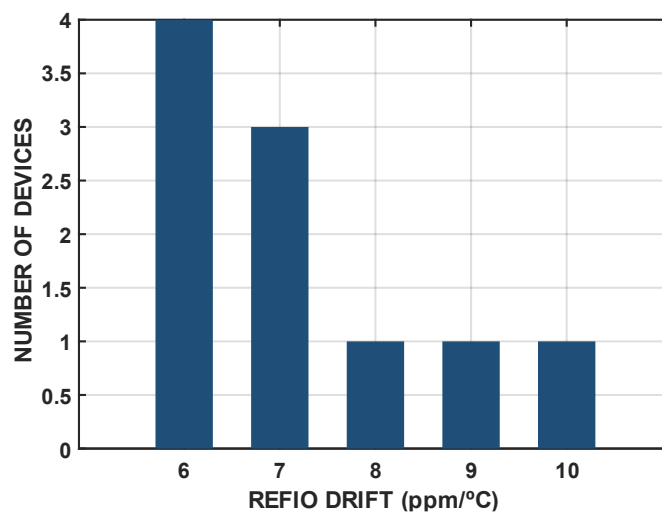


Figure 19 – Temperature drift of the voltage on the REFIO pin (from -40 to 125°)

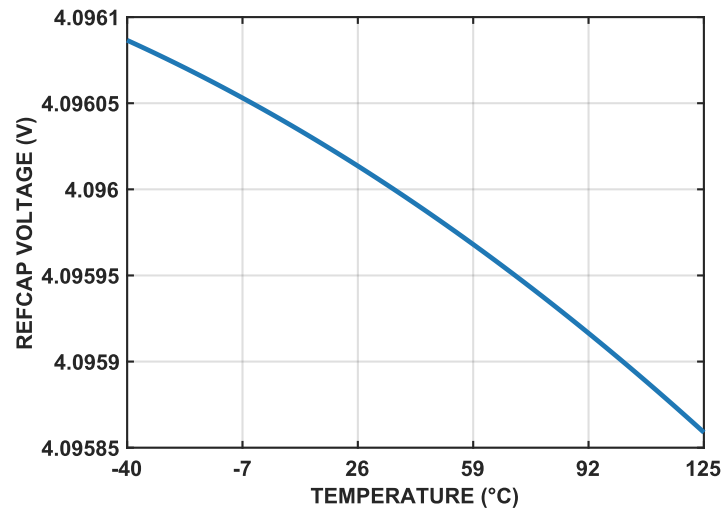


Figure 20 – Temperature dependence of the reference voltage buffer output (REFCAP)

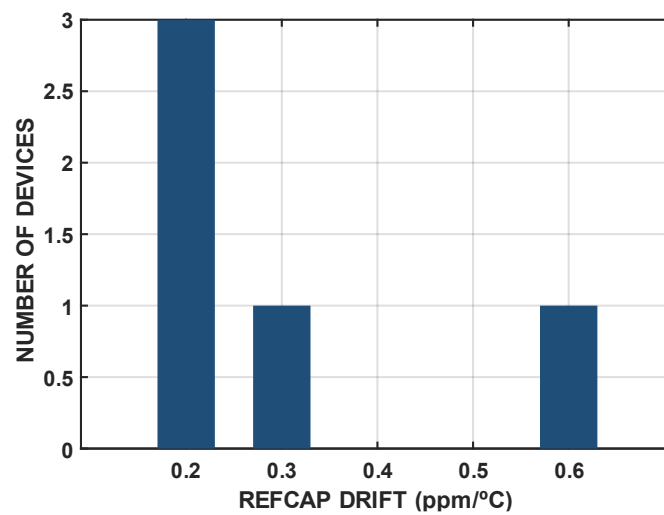


Figure 21 – Temperature drift of the voltage on the REFCAP pin (from -40 to 125°)

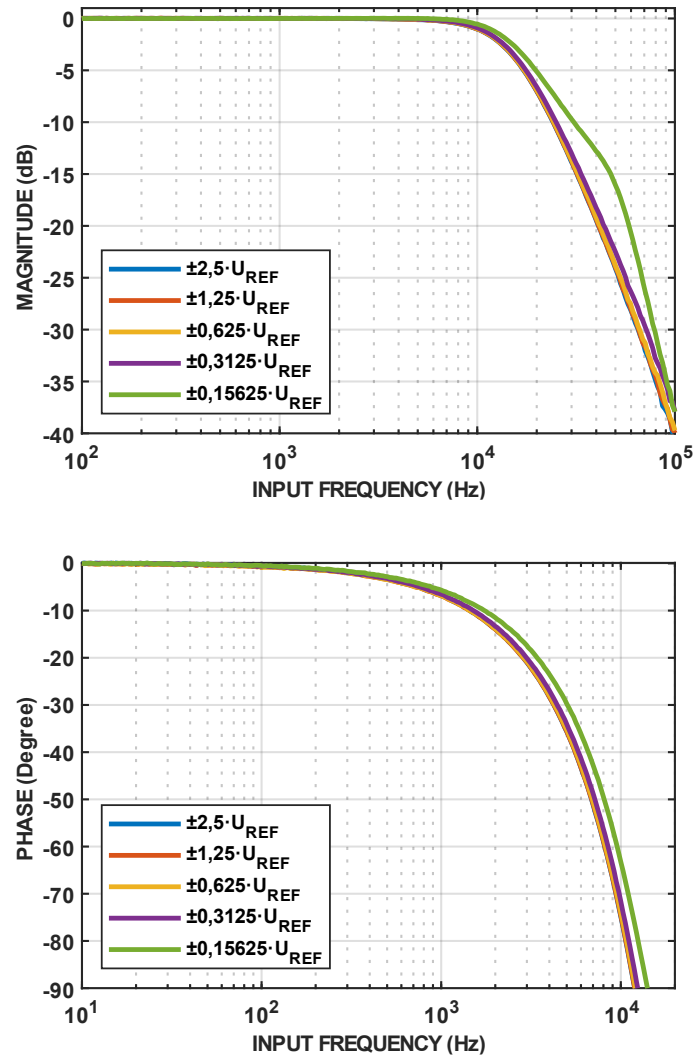


Figure 22 – Amplitude-frequency and phase--frequency characteristics of the channel for input ranges in nD=1 (single-ended), U=0 (bipolar) mode22

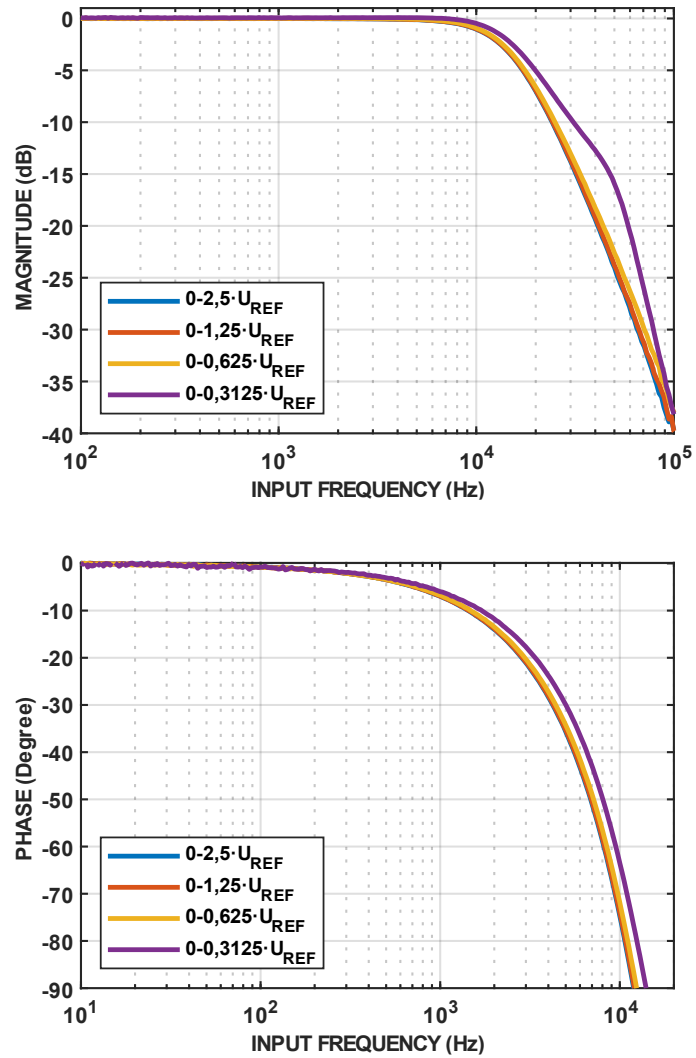


Figure 23 – Amplitude-frequency and phase-frequency characteristics of the channel for input ranges in nD=1 (single-ended), U=1 (unipolar) mode23

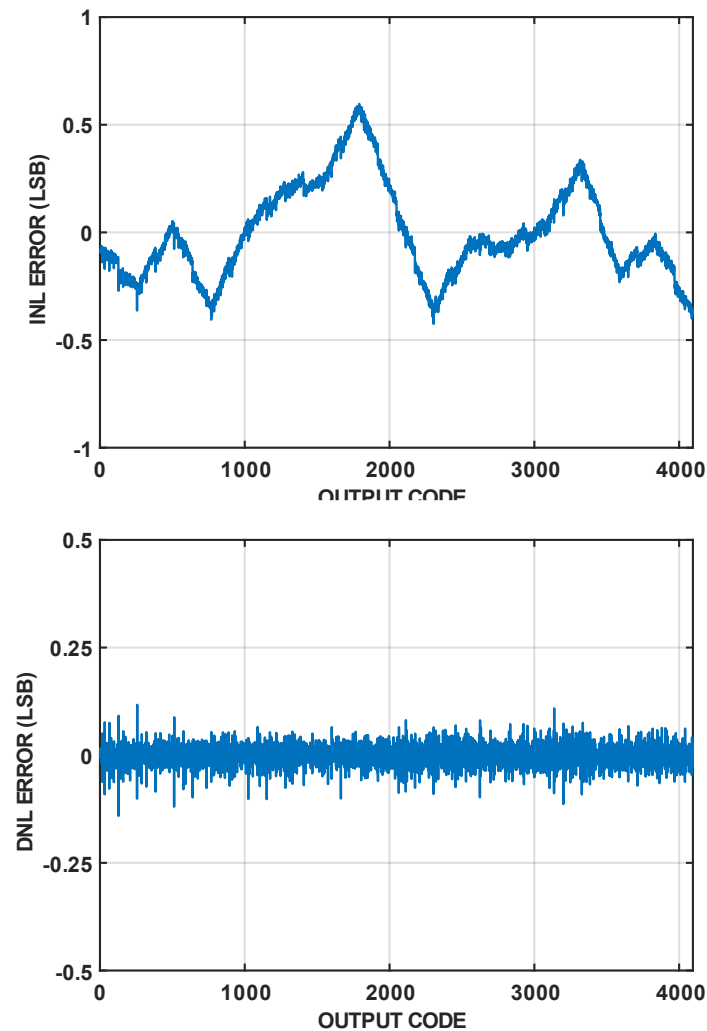


Figure 24 – Integral and differential nonlinearity, measured on channel 0 in GAIN=1 (± 5.12 V), nD=1 (single-ended), U=0 (bipolar)

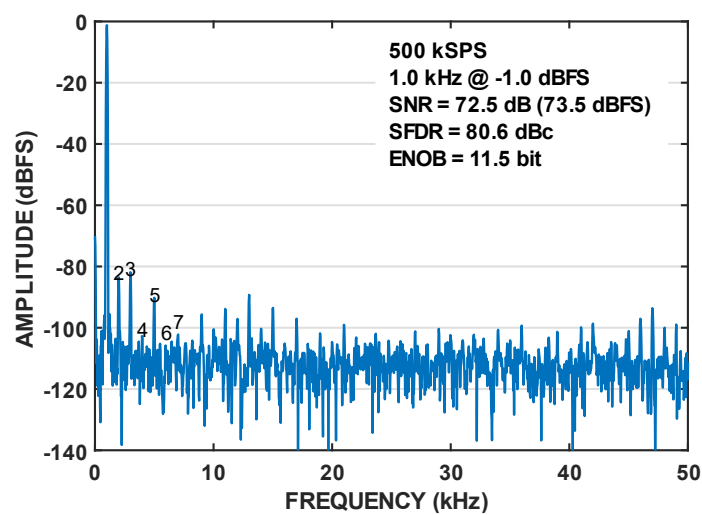


Figure 25 – Fragment of the output spectrum, measured on channel 0 in GAIN=1 (± 5.12 V), nD=1 (single-ended), U=0 (bipolar)

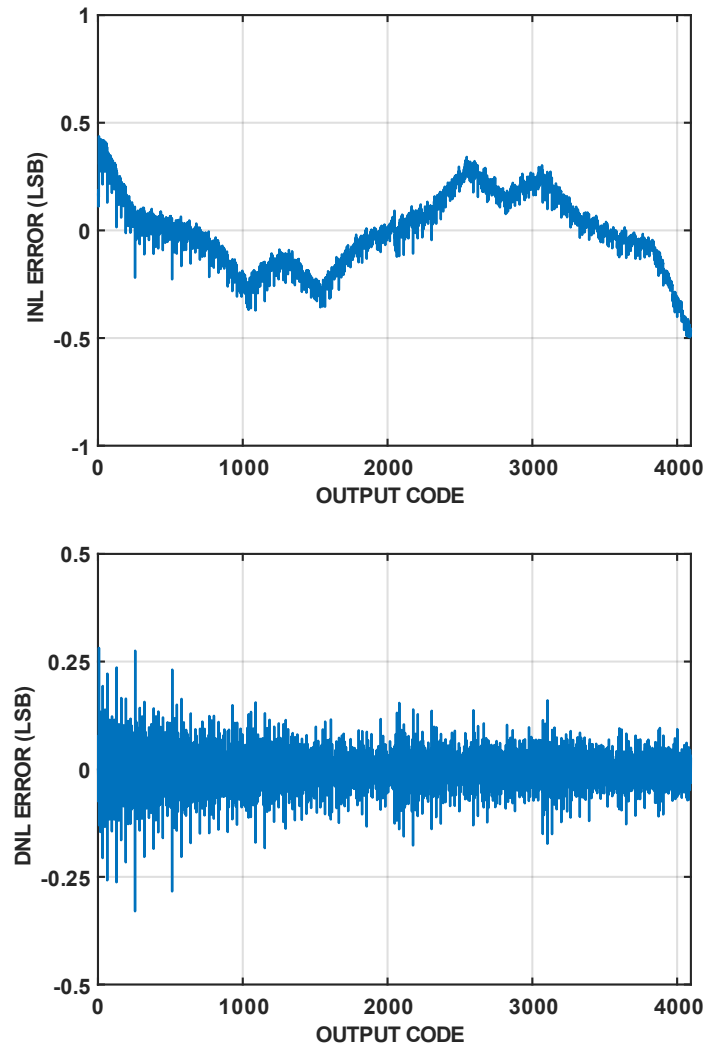


Figure 26 – Integral and differential nonlinearity in direct ADC access mode (AUX)

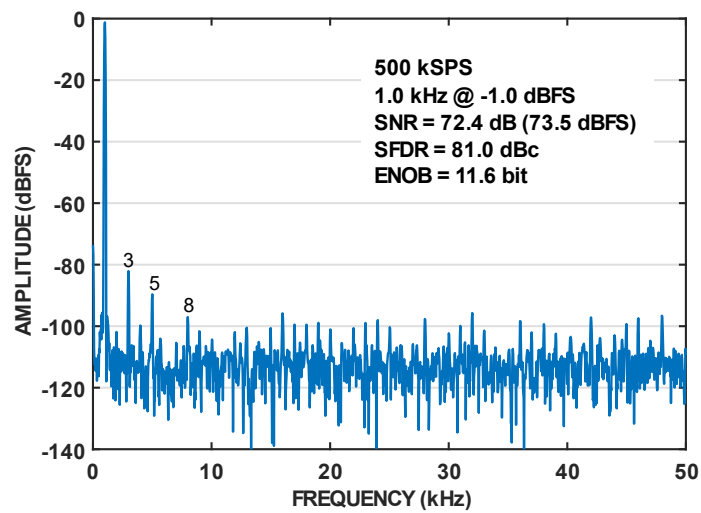


Figure 27 – Fragment of the output spectrum, measured in direct ADC access mode (AUX)

12 Outline drawing of the integrated circuit

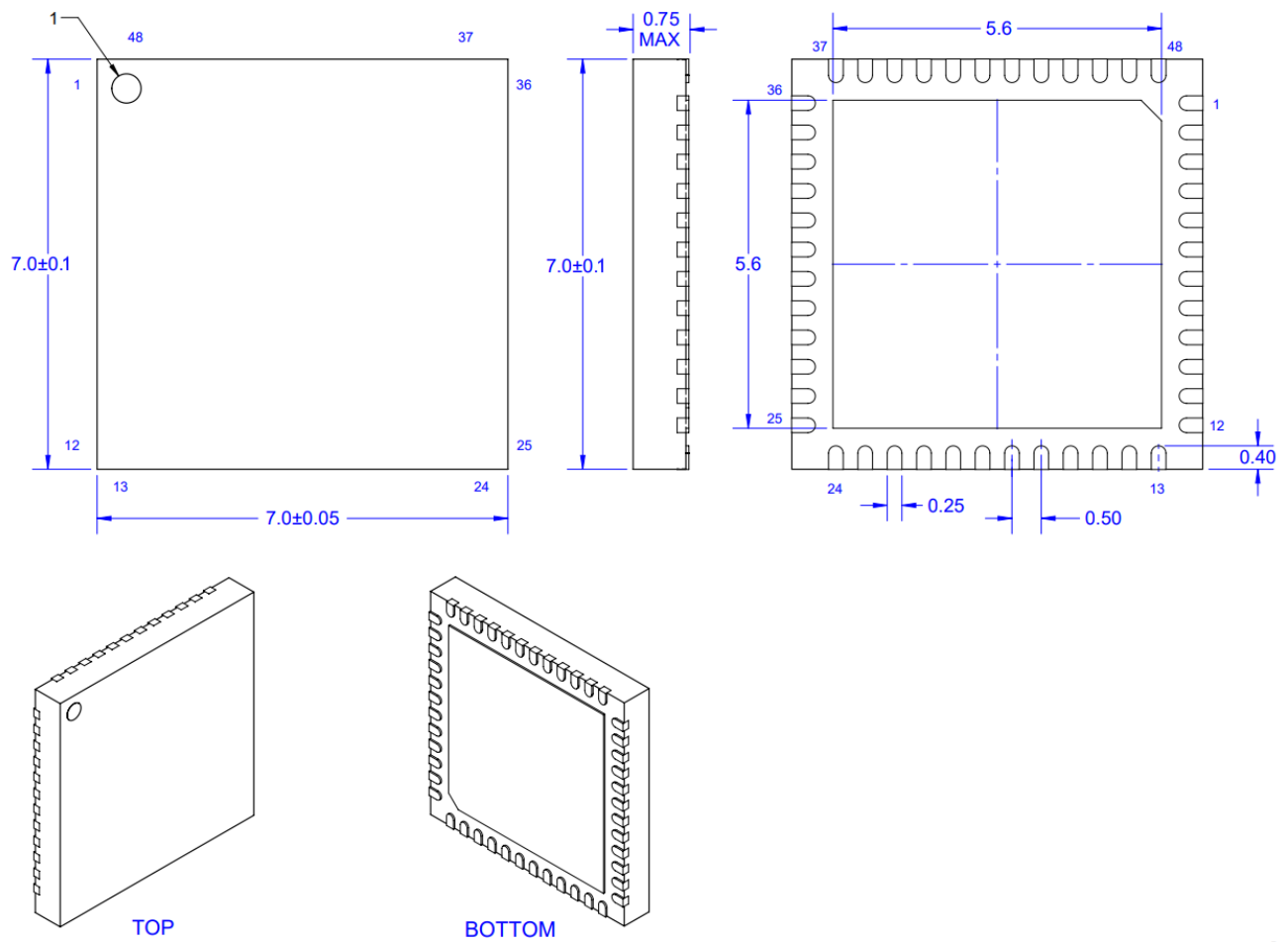


Figure 28 – Device in a 48-pin package QFN (7x7x0.75 mm)

[illegible]